IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TRANSMETA CORPORATION,	)	
	)	
Plaintiff,	)	
	)	
	)	
v.	)	C.A. No.06-633 (GMS)
	)	
INTEL CORPORATION,	)	**REDACTED**
	)	**PUBLIC VERSION**
Defendant.	)	

DECLARATION OF JOHN O'HARA HORSLEY

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Original Filing Date: August 17, 2007
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I, JOHN O'HARA HORSLEY, declare

1. I have personal knowledge of the matters set forth in this declaration and if called to testify I could and would competently testify to them.

2. I am currently the Executive Vice President, General Counsel and Secretary for Transmeta Corporation ("Transmeta"), based in Santa Clara, California. I joined Transmeta as its General Counsel in July 2000, and I have served continuously in that role and as an executive officer of Transmeta since that time. In addition to my responsibilities as General Counsel, I have served Transmeta in a variety of other management roles to meet the company's needs, including acting as Chief Financial Officer on an interim basis from June 2004 to September 2004, and actively supervising our Human Resources functions from July 2002 until February 2006.

3. Prior to joining Transmeta, from November 1997 to July 2000, I served at the Federal Trade Commission in Washington, D.C. as Deputy Assistant Director in appointed positions in the Bureau of Competition, most recently as Chief Counsel for Intellectual Property and Technology Matters. While at the FTC, I was responsible for merger review and antitrust enforcement in several technology industries, including semiconductors and computers. During my tenure at the FTC, I devoted substantial attention to analyzing economic conditions in the microprocessor and semiconductor industries, with a particular focus on industrial innovation and significant technological advances in those fields.

4. From October 1988 to October 1997, I practiced law as an associate and partner with Pillsbury Madison & Sutro, where I specialized in litigation and strategic counseling in intellectual property, antitrust and securities law and shareholder matters.

5. I earned a B.A. in Philosophy and a B.A. in English from the University of Utah, and a J.D. from the Boalt Hall School of Law at the University of California at Berkeley. At Boalt Hall, I served on the founding board of editors for the Berkeley Technology Law Journal (1985-86) and as Editor-in-Chief of the California Law Review (1987-88).

6. I first became aware of Transmeta in 1998 and followed Transmeta's public launch in early 2000. In my view, Transmeta was a highly innovative engineering company that, among other things, pioneered the way and created new customer expectations and demand for the inexpensive, energy efficient microprocessors used in today's mobile computing devices. Transmeta was founded in March 1995 with the mission of developing a new software-based microprocessor designed for highly efficient computing. Transmeta's microprocessors were and are unique because, unlike traditional microprocessors that are built entirely with silicon hardware, they integrate software and silicon hardware components in a unitary device. Transmeta's software component, which is called CodeMorphing software, dynamically translates the ones and zeros of software instructions into a functionally equivalent but simpler set of ones and zeros for decoding and execution by the silicon hardware component. CodeMorphing software also continuously "learns" about the programs run by a user and re-optimizes program execution for higher performance and reduced power usage. The silicon hardware component is a semiconductor chip with a relatively simple internal design, primarily optimized for speed and power efficiency. In Transmeta's processors, complex control and instruction scheduling functions, which are normally performed in silicon hardware, are instead handled by CodeMorphing software. By moving these functions from hardware into software, Transmeta was able to design and produce innovative microprocessor devices with fewer logic transistors, smaller die sizes, greater integration capacity, greater computing efficiency, and

substantial reductions in power consumption, waste heat generation, and system cooling requirements.

7. Transmeta worked in relative secrecy until January 19, 2000, when it announced its revolutionary Crusoe microprocessor. Transmeta's unique technology attracted corporate investment from several leading computer and technology companies, including AOL, Compaq, Gateway, IBM, Phoenix Technologies, Samsung, Sony and Toshiba.

8. With the launch of its Crusoe microprocessor, Transmeta entered the market for x86-compatible microprocessors – a market that Intel had dominated since the early 1980's, when IBM adopted Intel's 8086 microprocessor for its "IBM-PC" product. The term "x86" refers to the instruction set architecture that was first embodied in a series of Intel microprocessor devices with the product designations 8086, 80186, 80286, 80386, and etc.

9. Unlike the Intel microprocessors available at the time, the Transmeta Crusoe microprocessor was designed and promoted for its computing and energy efficiency, and was ideally suited for mobile computers and other computing applications that required low power consumption and thermal efficiency. In addition to the design advantages inherent in its software-based architecture, the Crusoe microprocessor featured an innovative adaptive power control technology that Transmeta called LongRun and claimed in the '061 patent in suit. Transmeta's LongRun technology increased the computing efficiency and reduced the power consumption of the Crusoe microprocessor, which enabled significant increases in the battery life of notebook computers.

10. Transmeta's innovative approach to microprocessor design attracted substantial public interest and extensive media coverage in both industry and general news publications. Much of the media coverage focused on the competitive challenges that

Transmeta's new technologies and products posed for Intel's microprocessor roadmap and historic market dominance. In this declaration, I have included a small sample of representative media stories that I personally read at or near the time of their original publication in 2000 and 2001.

11. Attached hereto as Exhibit 1 is a true and correct copy of a New York Times article entitled "New Design for Processor to Test Intel," dated January 20, 2000.

12. Attached hereto as Exhibit 2 is a true and correct copy of the cover story in the March 2000 issue of Red Herring, then the leading Silicon Valley technology publication, entitled "This Could Change Everything – Behind Transmeta's Bid to Power the Post-PC Era."

13. Attached hereto as Exhibit 3 is a true and correct copy of an article in The Wall Street Journal entitled "Transmeta Unveils New Chips in Ambitious Bid to Take on Intel," dated January 19, 2000.

14. Attached hereto as Exhibit 4 is a true and correct copy of a cover story in the February 2000 issue of Microprocessor Report, a leading publication of the microprocessor industry, entitled "Transmeta Breaks X86 Low Power Barrier."

15. Attached hereto as Exhibit 5 is a true and correct copy of a cover story in the July 2000 issue of Microprocessor Report, entitled "Top PC Vendors Adopt Crusoe."

16. Attached hereto as Exhibit 6 is a true and correct copy of an article in Business Week dated May 29, 2000, entitled "A Silicon Chameleon Challenges Intel."

17. In late June 2000, I attended the PC Expo trade show in New York City, which was then a major annual industry event. In the exposition hall, I saw demonstrations of advanced notebook computers from several PC manufacturers, including Fujitsu, Hitachi, and IBM, all featuring Transmeta's new Crusoe microprocessor. Transmeta's Crusoe

microprocessor won "Best of Show" at PC Expo 2000. I was impressed by those product demonstrations, which were material to my decision to join Transmeta as its General Counsel in July 2000.

18. In November 2000, Transmeta had its initial public offering, which raised \$273 million. Transmeta is a public company, and its common stock continues to be traded on the Nasdaq Global Market System.

19. By the end of 2001, Transmeta had a workforce of approximately 440 employees and contractors worldwide, including more than 300 engineers engaged in research and development in Santa Clara, California and Acton, Massachusetts.

20. By that time, the Crusoe microprocessor had been adopted by most of the leading Japanese computer manufacturers, primarily for applications in compact "ultra-light" notebook computers. Sales to the Japanese OEM computer manufacturers accounted for the vast majority of Transmeta's revenue during 2000, 2001 and 2002, and Transmeta's relationships with those customers were critical to Transmeta's credibility in the marketplace.

21. In February 2001, Transmeta acquired all rights to the Speculative Address Translation patents in suit from their original inventor, Richard Belgard, who was an advisor and consultant to Transmeta. The Speculative Address Translation patents include U.S. Patents Nos. 5,895,503; 6,226,733; 6,430,668 and 6,813,699, which are now in suit.

22. I represented Transmeta in negotiations with Mr. Belgard concerning his Speculative Address Translation patents. [redacted]

[redacted]

23. In June 2001, Transmeta and Seiko Epson Corporation jointly announced a strategic alliance relationship for the development of energy-saving microprocessor technologies. A true and correct copy of the English language announcement of that alliance is attached hereto as Exhibit 7. As part of their strategic relationship, Seiko Epson assigned to Transmeta certain patents and patent rights, including all rights in the then-issued Instruction Scheduling and Multiple Typed Register patents and their continuations. The Instruction Scheduling patents include U.S. Patents Nos. 5,737,624; 5,974,526 and 6,289,433, which are now in suit. The Multiple Typed Register patents include U.S. Patents Nos. 5,493,687; 5,838,986 and 6,044,449, which are now in suit.

24. I represented Transmeta in negotiations with Seiko Epson relating to the Instruction Scheduling and Multiple Typed Register patents in 2001. [redacted]

25. In August 2002, David M. Simon, then Intel's Director of Intellectual Property, contacted me to inquire about Transmeta's patent portfolio, including the patents that had been assigned to Transmeta by Seiko Epson and Richard. Belgard in 2001. Mr. Simon and I communicated intermittently between August and October 2002. Mr. Simon indicated that Intel was potentially interested both in a license under Transmeta's patents and in acquiring access to certain of Transmeta's advanced technologies. Mr. Simon also stated that Intel wished to avoid a patent dispute with Transmeta, and that a patent dispute would interfere with potential technology licensing or collaboration scenarios between the companies. I invited Mr. Simon to

consider Intel's staffing for a prospective meeting about Intel's interest in a potential technology exchange between the companies and to send an appropriate form of nondisclosure agreement. Intel did not provide a form of nondisclosure agreement at that time.

26. [redacted]

27. In October 2003, Transmeta introduced its second-generation product, the Efficeon microprocessor. The Efficeon microprocessor also used Transmeta's CodeMorphing software and LongRun power management technology, and featured architectural improvements that increased the performance range by more than 50% over the Crusoe microprocessor while still delivering significant power savings and thermal design efficiency in a small die size.

28. Intel undertook substantial efforts to undermine and discredit the launches and impact of Transmeta's Crusoe and Efficeon products. On January 18, 2000, a day before Transmeta's scheduled announcement of its Crusoe microprocessor with its power saving LongRun technology, Intel publicly announced its own inferior power saving feature called "SpeedStep." In 2000 and 2001, Intel then embarked on a crash program in an attempt to match LongRun, introducing new lines of low voltage microprocessor products specifically targeted for use in laptops and positioned against Transmeta, and later featuring LongRun-like adaptive power control technology that Intel called "Enhanced Intel SpeedStep Technology." Transmeta asserts in this action that Intel's Enhanced SpeedStep technology uses the adaptive power control

technology that Transmeta announced as LongRun in January 2000 and is covered by the '061 patent in suit.

29. I am informed and believe that beginning in 2002 Intel also resorted to a variety of aggressive and predatory business tactics to exclude Transmeta from dealing with its traditional Japanese OEM customer base. Intel's tactics included direct payments to computer manufacturers in return for exclusivity and near-exclusivity; discriminatory rebates, discounts and subsidies conditioned on customer "loyalty;" and threats of economic retaliation against companies who bought microprocessors from Transmeta or Advanced Micro Devices. Intel's exclusionary tactics in Japan disrupted Transmeta's relationships with all of its major Japanese OEM customers and effectively precluded any substantial sales of Transmeta's new Efficeon microprocessors in Japan.

30. Intel's tactics came to the attention of the Japan Fair Trade Commission (JFTC), which conducted surprise "dawn raids" collecting documents and information from Intel, Transmeta and other companies in April 2004. On March 8, 2005, after an investigation and subsequent enforcement proceedings, the JFTC recommended that Intel be sanctioned for its exclusionary misconduct directed at Transmeta and others. The JFTC ordered Intel to "cease and desist its conducts [sic] which violate Section 3 of the [Japan] Antimonopoly Act." The JFTC found that Intel "made the five major Japanese OEMs refrain from adopting competitors' CPUs" by offering discounts or rebates to deal exclusively with Intel. Attached hereto as Exhibit 8 is a true and correct copy of the JFTC's press release, dated March 8, 2005, concerning its findings and recommendations relating to Intel's business conduct in Japan.

31. Attached hereto as Exhibit 9 is a true and correct copy of a New York Times article dated March 9, 2005 and entitled "Japan Says Intel Violated Antimonopoly Law."

32. Intel agreed to comply with the JFTC's recommendations. Attached hereto as Exhibit 10 is a true and correct copy of an Intel press release dated March 31, 2005.

33. Unfortunately, the JFTC order came too late to reverse the damage that Intel's tactics had inflicted on Transmeta's business and its OEM customer relationships in Japan. During late 2004 and early 2005, Transmeta's management and Board of Directors assessed the economic and competitive conditions in the market for microprocessor products. Having spent more than $500 million to develop and build innovative microprocessors, and having accumulated a net deficit of $650 million at the end of 2004, Transmeta decided to begin the process of exiting the business of selling microprocessor products and put most of its products to End-of-Life status.

34. During the first quarter of 2005, Transmeta began modifying its business model to discontinue the manufacturing and sale of most of its microprocessor product lines and to further leverage its intellectual property rights and to increase its business focus on licensing its advanced power management and other proprietary technologies to other companies, and to provide microprocessor design and engineering services to other companies. Since March 2004, Transmeta has granted commercial licenses for certain of its advanced power management and semiconductor leakage control technologies to NEC Electronics, Fujitsu Limited, Sony Corporation and Toshiba Corporation.

35. Transmeta's discontinuation of its product lines forced it to reduce its workforce in 2005. By the end of 2005, Transmeta had a workforce of 221 employees, compared to a workforce of approximately 440 employees at the end of 2001. We did retain a fully integrated microprocessor development team of approximately 160 employees, and we continued advanced microprocessor development work, both on our own technology roadmap,

and on a proprietary project for Sony relating to a proprietary Sony microprocessor design. In 2005, Transmeta entered into two significant strategic alliance agreements with Sony and Microsoft to develop technologies and provide engineering services under contracts that scaled down over two years and expired by their terms upon completion in March 2007.

36. From August 2002 to January 2005, on a number of different occasions, Intel representatives approached Transmeta regarding potential technology collaborations with Transmeta. Substantive discussions between Intel and Transmeta were interrupted from time to time by various developments on both sides, including [redacted] the investigation and actions of the Japanese Fair Trade Commission described above in paragraph 30, and corporate reorganizations and management transitions at both companies

37. [redacted]

38. [redacted]

39. [redacted]

40. [redacted]

[redacted]

41. [redacted]

42. [redacted]

[redacted]

43. [redacted]

44. [redacted]

45. [redacted]

46. [redacted] Transmeta brought suit on October 11, 2006.

I declare under penalty of perjury that the foregoing is true and correct.

Executed on August 17, 2007

JOHN O'HARA HORSLEY

John O'Hara Horsley

CERTIFICATE OF SERVICE

I, the undersigned, hereby certify that on August 20, 2007, I electronically filed the foregoing with the Clerk of the Court using CM/ECF, which will send notification of such filing(s) to the following:

Josy W. Ingersoll

I also certify that copies were caused to be served on August 20, 2007, upon the following in the manner indicated:

BY HAND

Josy W. Ingersoll
John W. Shaw
YOUNG, CONAWAY, STARGATT & TAYLOR, LLP
The Brandywine Building
1000 West Street, 17th Flr.
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/s/ Richard J. Bauer (#4828)

Richard J. Bauer (#4828)

EXHIBIT 1

January 20, 2000

New Design for Processor to Test Intel

Transmeta Says Its Chip Can Run on Less Power

By JOHN MARKOFF

SARATOGA, Calif., Jan. 19 -- Ending almost five years of secrecy, the Transmeta Corporation announced a radical new microprocessor design today that promises tough competition for the Intel Corporation. The new chips are compatible with Intel's products while consuming substantially less power and costing less.

Transmeta's processors, by emphasizing software, are intended to improve on portable versions of Pentium-class microprocessors that power today's personal computers. The company said it was also pushing toward the widely anticipated post-PC era of mobile Internet computing.

Peter DaSilva for The New York Times

David Ditzel, founder and chief executive of Transmeta, holds a Web pad that runs on the company's new processor.

The chips are already being manufactured by the International Business Machines Corporation, which expects to begin shipping them by midyear.

In recent months Transmeta, a computer design company based in Santa Clara, Calif., has become the focus of widespread speculation in Silicon Valley, in part because of its well-kept secrecy and in part because its best-known employee is Linus Torvalds, the star

programmer who led the development of the free Linux operating system.

During a press event held here today at an upscale conference center in the foothills above Silicon Valley, Transmeta executives disclosed the first technical details of what they said was a fundamentally new and radical approach to microprocessor design.

With substantial support from I.B.M., Transmeta executives set the company on a strategic course that competes directly with Intel, the world's largest chip maker. The company has also both allied itself with the Microsoft Corporation and introduced products that will compete with Microsoft.

Analysts said today that I.B.M., which has committed itself to make Transmeta's chips at its semiconductor plant in Burlington, Vt., is making a big bet on the technology.

Transmeta's Crusoe chips, which take their name from the fictional character Robinson Crusoe and are intended for portable computing applications, are intended to drastically simplify computer hardware design by shifting complex operations to software that can be easily modified and quickly updated.

That approach puts the company on a different design path from Intel, which has created a more complex microprocessor family known as IA64 to press forward the next generation of computing.

Having raised about $100 million, with investors that include venture capital firms, the Microsoft co-founder Paul Allen's Vulcan Ventures, the George Soros Fund and Deutsche Bank, Transmeta is one of the largest gambles in years in Silicon Valley. It has 200 employees.

Today, the company's founder and chief executive, David R. Ditzel, said the company had kept a low profile in part because it wanted to protect its ideas and in part because it wanted to have a working product before it took its technology public.

He said the company was aiming first at the quickly growing mobile computing market, which many in the industry expect will accelerate when wireless Internet connections are easily available.

"The Internet changes everything," Mr. Ditzel said. "In the future you will no more want to leave your home without your Internet connection than you do without your cell phone today."

Mr. Ditzel founded Transmeta five years ago after leaving his position as chief scientist of Sun Microsystems' research

Related Articles
Intel Reports Strong Earnings

laboratories. He was also co-author of a computer science paper on the idea of RISC, or reduced instruction set computing, with David Patterson, a University of California computer scientist, in 1980.

RISC sought to change computing by shifting complexity from hardware to software, thereby streamlining chips and increasing their speed. Today, in an interview, Mr. Ditzel said that in a sense the Transmeta design was a return to the original RISC spirit.

At the heart of the new chip, however, is a processing core based around a technology known as V.L.I.W., or very long instruction word, which is also being embraced by Intel and Hewlett-Packard in the new IA64 chip. V.L.I.W. tries to speed up computing by executing many simple instructions in parallel.

The company said its top-of-the-line chip, the TM5400, would have a clock speed of 700 MHz and would consume, on average, about one watt of power, far lower than today's low-power Intel chips, which can consume 10 watts or more. That chip is intended for subnotebook portable computers that run Microsoft's Windows operating system.

(January 14, 2000)

Intel Falls After Downgrade
(November 12, 1999)

AMD to Raise Speed Bar With 700-Mhz Athlon
(October 2, 1999)

Intel Reduces Prices on Pentium III Chips
(August 24, 1999)

Advanced Micro to Introduce Faster Chip
(August 10, 1999)

Intel Will Raise the Ante in Chip-Manufacturing Technology
(June 10, 1999)

New Chip May Make Today's Computer Passe
(September 17, 1997)

The Demise of Moore's Law Signals the Digital Frontier's End
(August 14, 1996)

A second Transmeta chip, the TM3120, has a clock speed of 400 MHz, consumes about one watt and is intended for Internet network appliances that run a version of the Linux operating system.

"We have a great relationship with Microsoft," Mr. Ditzel said. "It's kind of like, 'Let the best software win.'"

Today, a spokesman for Intel said the giant chip maker would not comment on Transmeta, which is situated only a few blocks from Intel's headquarters in Santa Clara.

Transmeta produced several demonstrations today showing the use of a software technology named LongRun, which is intended to dynamically adjust the speed of a microprocessor to consume less power as it learns about the characteristics of a particular application.

In one demonstration, the company showed its chip running a DVD

movie while consuming only a fraction of the power drawn by a comparable Intel chip.

The major difference between processors from Intel and Transmeta is Transmeta's decision to rely mostly on software both for emulating Intel's chips and for power management.

Transmeta's software technique, called code-morphing software, converts Intel computing instructions into V.L.I.W. instructions on the fly, sacrificing little performance.

At today's briefing, analysts pressed the company to provide specific performance benchmarks, which were not included in the press materials. Transmeta officials said that a high-end Transmeta chip would perform about as fast as a 500 MHz Pentium III microprocessor and that a computing system based on a Transmeta chip and its LongRun power management software would have battery life about twice as long as a comparable Intel system.

Mr. Torvalds said he had helped design the code-morphing approach and had worked on a special version of mobile Linux the company would use for network appliances.

The company did not announce specific products or customers today but said computer makers in the United States and Japan were planning to build computers based on the technology. A Compaq executive at today's event said his company was "interested" in Transmeta's chips.

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EXHIBIT 2

SPECIAL REPORT: THE NET AND SMALL BUSINESS

RED HERRING

THE BUSINESS OF TECHNOLOGY

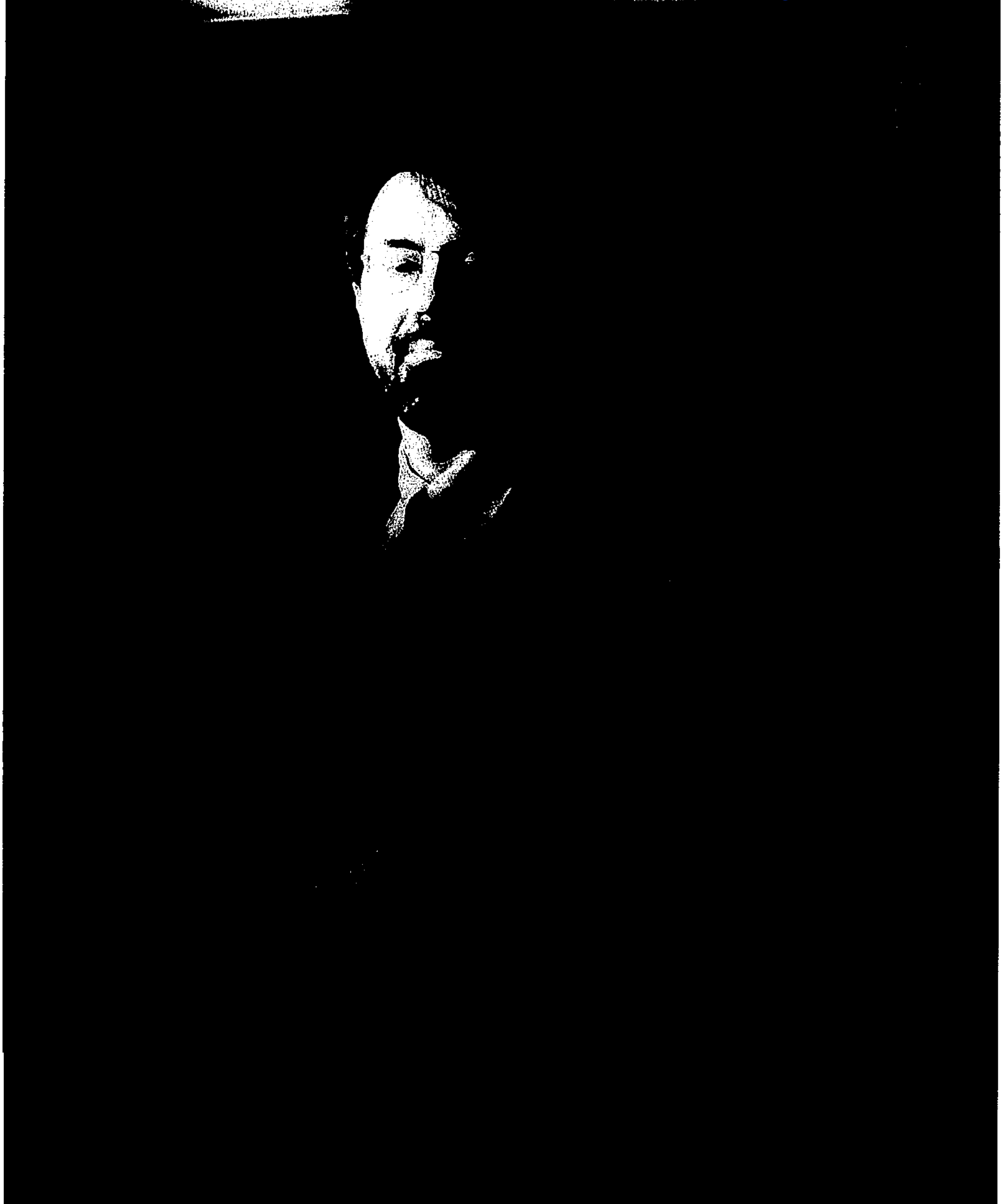
THIS COULD CHANGE EVERYTHING

Behind Transmeta's bid to power the post-PC era.

03>

RH NO 76
MARCH 2000
$4.99 U.S.
$6.99 CANADA

(The Crusoe chip, actual size) 



DAY CHIPPER. Cofounder and CEO of Transmeta, David Ditzel.

The upstart chip maker bets it all on a mobile, post-PC era.

By Justin Hibbard

BIG GAMBLE

On a few historic occasions, high-tech companies have placed enormous bets on a technology that could transform an industry—or fail spectacularly. In 1984 Apple Computer risked its future on the Macintosh and changed computing. Three years later, GO Corporation tried to convert the world to pen computing and wound up losing $75 million. Now comes Silicon Valley's latest

high-stakes gamble—Transmeta Corporation.

Five years and more than $100 million in the making, Transmeta was conceived in the tradition of Silicon Valley's legendary firms. Like Intel, Apple, and Sun Microsystems, it aims to build not just a company, but also a technology platform from which thousands of businesses might rise. "With a company like this, you're trying to create a new industry," says William Tai, a Transmeta board member and partner at Institutional Venture Partners.

Transmeta's product is a microprocessor, the brain that controls a computer. But this microprocessor is designed for a new era in which portable devices will supplant desktop PCs as the most common means of connecting to the Internet. These devices will give rise to Internet applications not limited by location or by the PC's deskbound, document-centric metaphors. Voice and data will be available anywhere and anytime, via handheld computers, cellular phones, and devices not yet invented, changing the way people live and work.

No one knows when—or whether—this era will arrive. But one factor that could help it arrive soon is a standard platform. The PC prevailed because Microsoft and Intel built a platform on which an army of PC makers and software developers built compatible products. Transmeta proposes a standard platform on which mobile device makers and Internet software developers can build products for the post-PC era.

The company faces tough competition from other chip makers, especially Intel. When Transmeta started in 1995, Intel's mobile processors consistently lagged behind its desktop processors in performance, leaving it vulnerable to competition from mobile specialists. Since then, Intel claims it has closed the gap between its mobile and desktop products. Last year, the company acquired StrongARM, a low-power chip for small devices. Now the burden is on Transmeta to differentiate its products from Intel's.

Transmeta's chief differentiator is its processor architecture. Unlike most processors, which consist almost entirely of silicon, Crusoe processors are half hardware and half software. By using software to do much of what chip hardware

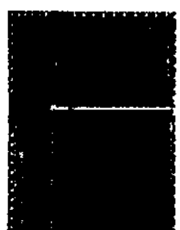
THE NEW CHIPS WERE NAMED AFTER ROBINSON CRUSOE, THE FICTIONAL ADVENTURER. BUT **CRUSOE ALSO BRINGS TO MIND A SHIPWRECK.** DANIEL DEFOE'S HERO SPENT 28 YEARS STRANDED ON A DESERT ISLAND.

TRANSMUTATION

The evolution of Transmeta, from a rebellion against complexity to one of the most anticipated technology releases of the new millennium.

1978
Bill Joy, future cofounder of Sun Microsystems, studies computer science at U.C. Berkeley alongside David Ditzel, future Sun employee and cofounder of Transmeta.

1980
David Patterson, a U.C. Berkeley professor, coauthors "The Case for the Reduced Instruction Set Computer" with former student David Ditzel, introducing the RISC processor to the world.

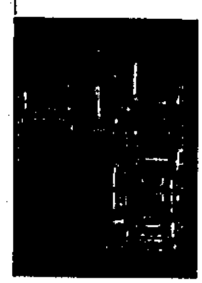


1982
David Patterson and researchers at U.C. Berkeley produce the RISC-I, an early RISC processor.

1986
Colin Hunter, future cofounder of Transmeta, founds Hunter Systems, which makes software that translates DOS applications to Unix.

1987
David Ditzel joins Sun Microsystems' SPARC technology group.

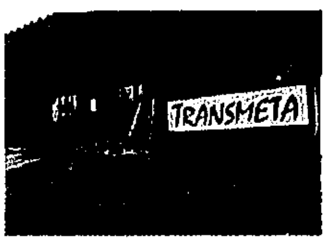
1988
AT&T designs the Hobbit processor for Apple's Newton handheld computer. The Hobbit is based on the CRISP, a RISC processor codesigned by David Ditzel.



WILLIAM MERCER MCLEOD

DOC TO THE SYSTEM: The presence of Linux inventor Linus Torvalds on the Transmeta technology development team brought heightened interest to the company.

1992
At Sun, David Ditzel forms a partnership with Russian computer scientist Boris Babaian.



MARCH 1995
David Ditzel, Doug Laird, Steve Goldstein, and Colin Hunter found Transmeta.

DECEMBER 1995
William Tai, partner at Walden Venture Capital, leads Transmeta's first round of financing ($5.5 million). Coinvestor: Institutional Venture Partners.

1997
William Tai, now a partner at Institutional Venture Partners, leads Transmeta's second round of financing ($15.4 million). Coinvestors: Vulcan Ventures, Integral Capital Partners, Novus Ventures, Walden Venture Capital.

1998
Transmeta produces the first sample of its microprocessor at IBM Microelectronics' foundry.

2000
Transmeta introduces its Crusoe line of processors.

METALLURGIST: David Ditzel's vision for what would become Transmeta extends back to his school days at the University of California at Berkeley.

usually does, the Crusoe processors are smaller, less expensive, and consume less power than conventional processors.

MY CHIP FRIDAY

The new chips were named after Robinson Crusoe, the fictional adventurer who sailed the Pacific. "Crusoe has a metaphor of mobility and travel," says James Chapman, Transmeta's vice president of marketing. But Crusoe also brings to mind a shipwreck. Daniel Defoe's hero spent 28 years stranded on a desert island.

Long before Transmeta introduced its platform, the company attracted extraordinary attention, for three things: its star software engineer, Linus Torvalds, creator of the Linux operating system; high-flying investors like Paul Allen and George Soros; and secrecy worthy of the CIA.

The company broke its five-year silence on January 19 when it introduced Crusoe in a historic villa in the foothills of the Santa Cruz Mountains. The headliner was David Ditzel, the gregarious cofounder and CEO with a knack for recruiting star engineers. Mr. Torvalds made a cameo appearance to demonstrate a Crusoe-powered machine by playing Quake against one of its creators, Dave Taylor, another Transmeta engineer. (Mr. Torvalds got slaughtered.)

There are two Crusoe processors, one for notebooks,

MR. DITZEL AND MR. PATTERSON'S RISC PAPER PROPOSED WHAT WAS THEN A **RADICAL IDEA**: ENGINEERS COULD MAKE A PROCESSOR RUN FASTER BY REDUCING THE NUMBER OF INSTRUCTIONS FED TO IT.

WILLIAM MERCER MCLEOD

the other for Internet appliances—anything smaller than a notebook and larger than a palm-top. Transmeta claims both chips consume about one watt of electricity on average, allowing a notebook to run all day on one battery. The appliance chip runs at 400 MHz, and the notebook chip at 700 MHz. The notebook chip runs Windows applications about as fast as Intel's 500-MHz mobile Pentium III, Transmeta says.

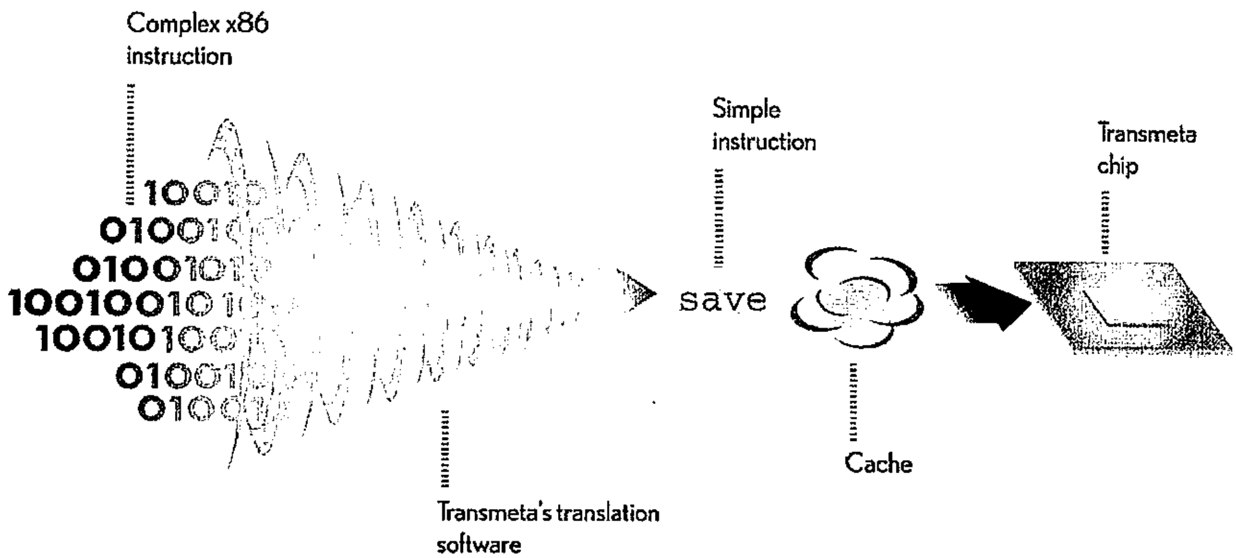
At its product launch, Transmeta declined to name companies using its chips in their products. But executives said Crusoe-based products will be introduced throughout this year. The company has designed specifications for several products that use its chips, including a tablet computer that connects to the Internet using wireless technology.

During the event, Mr. Ditzel explained how Transmeta will ensure that software programs written for Intel chips run on Transmeta's chips—an unofficial requirement to compete in the microprocessor business. Every chip has its own set of instructions that software programs use to make computers do things like save and print. Software companies must write different versions of their programs for each chip

'WE REALIZED THERE WERE LESS THAN A DOZEN PEOPLE IN THE WORLD CAPABLE OF BUILDING **SOFTWARE-BASED MICROPROCESSORS**. WE HAD ONE SIMPLE PLAN: HIRE ALL OF THEM.'

MIGHTY MORPHIN POWER SAVER

The process behind Transmeta's new microprocessor, Crusoe.



ZIP CODE: Every model of microprocessor has a unique set of instructions it can follow. Instructions are built into a processor, and software programs can call instructions to make a computer do things like save files, print files, and display graphics. Programs written for one processor's instruction set cannot run on another processor. But emulation software like Transmeta's code-morphing software can translate instructions written for one processor to instructions that will run on another one.

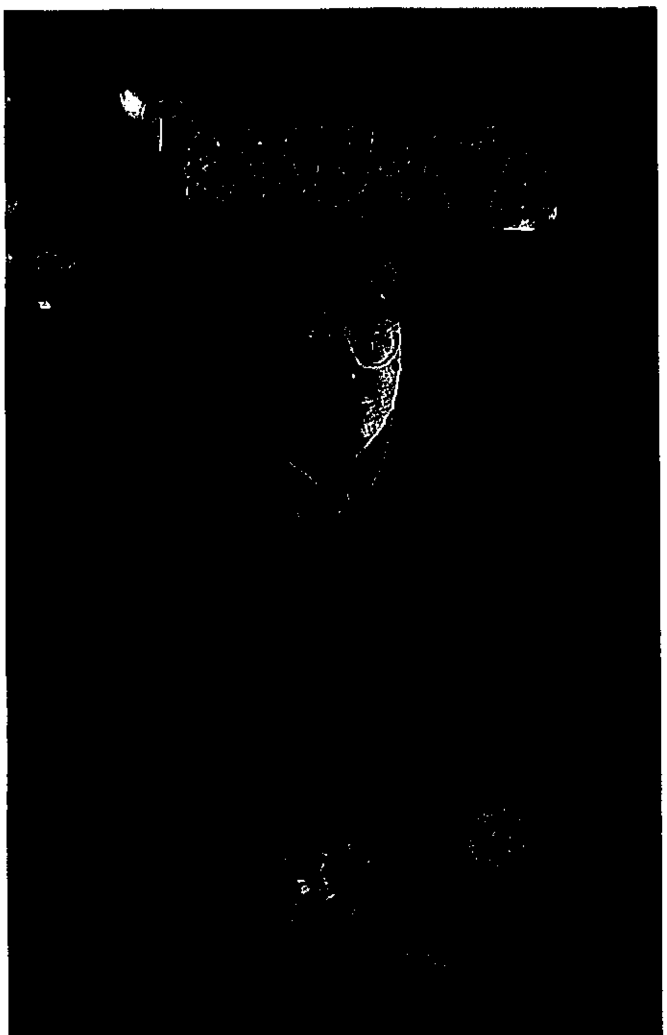
Transmeta's code-morphing software works together with the Crusoe processor hardware to translate foreign instruction sets, such as Intel's x86, into instructions for the Crusoe processor. The Crusoe instructions are in VLIW (Very Long Instruction Word) format, which groups several instructions together and processes them simultaneously, resulting in fast processing. The code-morphing software also works with the Crusoe processor hardware to reorder and reschedule the sequence in which the translated instructions are processed, optimizing them for faster performance. Translated instructions are stored in cache memory so that they can be recalled without translating, reordering, and rescheduling them again.

at considerable time and expense. Few of them will write programs for a new chip with little market share and little hope of capturing a market that Intel owns. But thousands of companies have written programs for Intel's instruction set, called x86. To run those programs, other chips must support x86, too.

'YOU'VE GOT TO HAVE A NICHE WHERE INTEL CANNOT COMPETE, AND THAT WAS **THE WHOLE IDEA BEHIND TRANSMETA**. INTEL CANNOT HAVE THE POWER AND PERFORMANCE OF TRANSMETA AT THE SAME TIME.'

The x86 instruction set has grown complex over the years, requiring more transistors, which consume more power. Moreover, when chip makers copy patented portions of Intel's chip design, they must pay licensing fees or battle Intel in court.

One of Transmeta's breakthroughs is what it calls "code-morphing software," which translates x86 instructions into instructions that Crusoe chips can process. By using software, rather than hardware, to do the translation, Transmeta can build a small, inexpensive, low-power chip that runs Windows applications—and avoid licensing fees and lawsuits. "I'm pretty sure that Transmeta is out of the woods on most of those patents," says Richard Belgard, an independent consultant who has studied Transmeta's patent filings.



TRANSMEDIATOR: Transmeta's new microprocessor will run Linus Torvalds's Linux operating system.

A software-based microprocessor is easier to repair and improve than a hardware-based one. Changing instructions in traditional chip hardware can take up to a year. Transmeta can change instructions in its software in a day and send the changes to a customer over the Internet. Or Transmeta can rapidly replace an instruction set. The company could even build several instruction sets into its software, allowing people to use applications for Windows, Macintosh, Unix, and Linux on one machine.

In theory, changes to Transmeta's software could improve the processor's performance. The company could sell the same chip hardware with two versions of software, one designed for greater speed than the other and each priced accordingly. To upgrade a processor, users could simply enter a credit card number on a Web site and download software. "The marketing possibilities are astonishing," says George Sarlo, a partner at Walden Venture Capital, a Transmeta investor. Whether manufacturers who use Transmeta's chip in their computers will want to control the software distribution remains to be seen.

CALCULATED RISC

Transmeta is not Mr. Ditzel's first effort to simplify microprocessors through the use of software. In fact, his efforts began 20 years ago. In 1978 he earned his master's degree in computer science from the University of California at Berkeley, where he studied alongside future stars like Eric Schmidt and Bill Joy, cofounders of Sun Microsystems. In 1980, while working as a chip designer at AT&T's Bell Labs, he collaborated on a paper with one of his Berkeley professors, David Patterson. "The Case for the Reduced Instruction Set Computer" proposed what was then a radical idea: engineers could make a processor run faster by reducing the number of instructions fed to it.

An obscure technical newsletter published the paper, and the Reduced Instruction Set Computer (RISC) quickly won fans throughout the engineering community. But it was heretical to engineers who believed in a conventional approach called the Complex Instruction Set Computer, or

WILLIAM MERCER MCLEOD

ALCHEMICAL COMPOUND: The Santa Clara, California headquarters of Transmeta, until now shrouded in mystery.

CISC, which uses elaborate instructions and requires complex circuitry. CISC devotees soon published a rebuttal, and what became known as the RISC/CISC debate began.

Within ten years, this esoteric dispute had escalated to a holy war that pitted multibillion-dollar corporations against one another, and divided the computer industry into two factions. By the 1990s, companies like Sun, Hewlett-Packard, IBM, Motorola, and Apple had staked their businesses on RISC. Intel and Microsoft had built a PC empire based on CISC. The Macintosh versus the PC, Windows versus Unix, the Pentium processor versus the PowerPC processor—all these rivalries stemmed from "The Case for the Reduced Instruction Set Computer."

Mr. Ditzel proved to be not only a gifted scientist but also an effective spokesman for his ideas. In 1982 he organized one of the first conferences that featured a RISC/CISC debate. He persuaded IBM to let one of its researchers speak at the conference about RISC technology the company had been quietly developing since 1976. Mr. Ditzel's gift for persuading other scientists to join his causes would become a hallmark of his career, as evidenced by the top-ranked engineers he attracted to Transmeta. "Dave is the world's best recruiter," says Mr. Patterson, his coauthor on the RISC paper.

'I WENT BACK TO MY HOTEL IN THE EVENING, AND I THOUGHT, **THESE PEOPLE ARE CRAZY**. I STILL HAVEN'T SEEN A COMPANY DOING ANYTHING AS EXCITING AS TRANSMETA.'

While promoting RISC in the engineering world, Mr. Ditzel was helping design a RISC processor inside AT&T, called the C-language Reduced Instruction Set Processor (CRISP). CRISP was never released, but the design became the basis for the Hobbit, a low-power RISC chip that AT&T developed in 1988 for handheld

JASON GROW

computers. Foreshadowing Transmeta, AT&T was one of the first companies to see that it could exploit the simple circuitry of a RISC processor to produce a chip that consumed little battery power.

In 1987 Mr. Ditzel joined Sun, where he worked for eight years as an architect and spokesman for scalable processor architecture (SPARC), the RISC design underlying Sun's processors. Eventually, he joined the growing number of engineers who believed microprocessors were becoming too complex. Even RISC processors, designed originally for simplicity, were gaining more and more transistors. Mr. Ditzel started thinking about how to simplify processors. He decided software was the answer.

'TARGETING MOBILE DEVICES AND INFORMATION APPLIANCES IS SMART. **TRANSMETA HAS RECOGNIZED** THAT TRYING TO DUKE IT OUT IN THE DESKTOP SPACE IS A LOSING PROPOSITION.'

CENTRAL PROCESSOR: Mr. Ditzel is betting a simpler, faster, less power-hungry chip will dominate the mobile computing world

Transmeta was incorporated on March 3, 1995, to bring forth Mr. Ditzel's vision of building software-based microprocessors. He went to work recruiting engineers who could pull off the technological feat. "We realized there were less than a dozen people in the world capable of doing this," Mr. Ditzel says. "We had one simple plan: hire all of them." And Transmeta did—not only to gain their expertise but also to keep them out of competitors' ranks.

TRANSFIXED

The first venture capital firm to invest in Transmeta was Walden Venture Capital. The firm saw an opportunity for Transmeta in the mobile computing market, where Intel seemed more vulnerable than in the desktop market. "You've got to have a niche where Intel cannot compete, and that was the whole idea behind Transmeta," says George Sarlo, a partner at Walden. "It was physically impossible for Intel to have the power and the performance of Transmeta at the same time." Walden brought Institutional Venture Partners into the deal, and in December 1995 the firms invested a total of about $5.5 million in Transmeta.

By 1997 Transmeta had a commitment from IBM to manufacture its chips and provide technical support. The deal helped Transmeta attract a new cadre of prestigious investors. In April 1997, the company closed a $15 million round of financing that included participants like Vulcan Ventures (the VC operation of Microsoft cofounder Paul Allen), Integral Capital Partners, and, once again, Institutional Venture Partners and Walden, who also brought in Novus Ventures.

Also in 1997, Transmeta hired Linus Torvalds, the creator of Linux. At the time, Mr. Torvalds had several job offers, many of them from Linux companies. On his first visit to Transmeta, he toured the company for a day. "I went back to my hotel in the evening, and I thought, 'these people are crazy,'" he says. "When I came in the next day, I had decided that if I was going to work for a company, I wanted to work for a company that was doing something fun and interesting. I still haven't seen anything as exciting as Transmeta."

Though Mr. Torvalds was known as the ultimate authority on Linux, Transmeta hired him for his general

WILLIAM MERCER MCLEOD

software engineering skills. He worked on Transmeta's code-morphing software.

SLOW METABOLISM

In January 1998, Transmeta produced the first prototype of its processor at IBM Microelectronics' foundry. The chip did not perform at the level the company had expected—not unusual for a prototype. According to a former Transmeta engineer, the company thought its processor would run x86 applications at speeds comparable to a 400-MHz Pentium II. Instead, it ran them about as fast as a 200-MHz Pentium I. Other aspects of the chip met expectations—it consumed little power, and it translated instructions accurately. Transmeta's engineers went to work fixing the bugs and improved the performance.

'PEOPLE BUY LAPTOPS WITH A VERY CLEAR FOCUS ON THE CLOCK SPEED. BUT **PEOPLE DON'T DO THAT WITH PORTABLE DEVICES**. PEOPLE DON'T CARE WHAT KIND OF CHIPS ARE IN THE MACHINES.'

Mr. Ditzel dismisses the incident as a mere test. But some insiders say it led Transmeta to refocus its target market. "There was a time when we thought the promise of the architecture was powerful enough that we could go after almost every market," says William Tai, a Transmeta board member and partner at Institutional Venture Partners. "But we realized we couldn't do everything. So we dug down in our roots and said, 'What are we really good at?'" Given Transmeta's low power consumption, the answer was mobile Internet devices.

To be sure, the company squeezed the best performance it could get out of its chips. But speed comes at the expense of low power, and Transmeta had to decide which feature to emphasize. It went with its strength—low power. The firm still claims its chips perform competitively. But Transmeta has called for a new methods of measuring the performance of mobile chips that give more weight to power consumption.

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Mr. Ditzel places the company's decision to focus on mobile devices at an earlier date. "We had toyed with the idea of doing desktops," Mr. Ditzel says. "As we came to understand the technology, we realized mobile was best." A turning point, he says, came in 1997 when Transmeta discovered that it could cut power consumption by as much as 50 percent by programming its processor to learn which parts of a program a person uses most and optimize those parts to run most efficiently. That discovery, Mr. Ditzel says, showed Transmeta where its strength were.

Transmeta's strength happens to coincide with a market poised to boom. The number of mobile devices sold worldwide will jump from 3.9 million in 1998 to 21.3 million in 2003, according to market research firm Dataquest. That's still fewer than the 199 million PCs that Dataquest predicts will sell worldwide in 2003. But sales of mobile devices are growing at a compound annual rate of 45 percent, while PC sales are growing at 22 percent.

"Targeting mobile devices and information appliances, which have tremendous upside potential, is smart," says David Hayden, an analyst at Mobile Insights. "Transmeta has recognized that trying to duke it out in the desktop space is a losing proposition."

Intel, king of the desktop, has its eye on the mobile market, too. Unlike five years ago when Transmeta was founded, Intel's mobile processors no longer trail its desktop processors in performance. In January, Intel introduced its 650-MHz mobile Pentium III processor with new power management technology. It was the third increase in mobile processor speed that Intel had introduced within a year, nearly doubling the speed it offered a year earlier.

Speed continues to drive sales of PCs. But in a new world of mobile Internet devices, there's no guarantee users will value performance over other criteria, like price and battery life. "People buy laptops with a very clear focus on the clock speed," says Joseph Osha, an analyst at Merrill Lynch. "But people don't do that with portable devices. In a new market, people don't care what kind of chips are in the machines."

In the sort term, that may be good for Transmeta. It means there is an opportunity for an upstart chip maker to distribute its chips widely in a new class of devices. But eventually, it will serve Transmeta well if people care whether a Crusoe processor is in their device. And it will serve the burgeoning mobile Internet device industry to have a standard platform on which devices and applications are based.

A standard mobile Internet platform will promote the development of Internet applications that go beyond PC functionality. Current Internet applications are based on features that have been used in PCs for more than 20 years. Web pages, for example, are relics of the document metaphor used in early PC graphical user interfaces in the 1970s. When the Internet is available through small devices that can roam anywhere, applications will emerge that we haven't yet imagined.

Even if Transmeta doesn't bring these applications into the world, it shows us that they are possible.

Write to justin@redherring.com. Red Herring Online reporters Larry Aragon and Phil Harvey, and Red Herring *research associate Tom Geck contributed to this story.*

EXHIBIT 3

THE WALL STREET JOURNAL INTERACTIVE EDITION FROM THE ARCHIVES

January 19, 2000

Transmeta Unveils New Chips In Ambitious Bid to Take on Intel

By DEAN TAKAHASHI
Staff Reporter of THE WALL STREET JOURNAL

SANTA CLARA, Calif. -- Transmeta Corp. unveiled a new kind of chip for portable computers Wednesday, a move that could deliver huge benefits to consumers of these products -- and possibly transform Transmeta into a threat to market leader Intel Corp.

David Ditzel, chief executive of the secretive Silicon Valley start-up (www.transmeta.com), showed a number of personal computers using the company's "Crusoe" family of microprocessors. The chips can run Microsoft Corp.'s Windows operating-system software just like Intel's chips do, but they can also run other operating systems, such as Linux.

"We're going after the x86 [Intel-compatible] market and can run any kind of x86 out there," Mr. Ditzel said in an interview before the announcement. "We're going into mobile Internet computers, and we're creating a whole new category of computing."

Transmeta's chips use patented "code-morphing" software to translate Windows or Linux software instructions into a native code that the Crusoe chips can efficiently process. Hence, Transmeta uses generic hardware chips that are tailored by the software to run either Windows, Linux or Sun Microsystems Inc.'s Java. Because the chips rely upon the translation software for many functions, the actual hardware of the chips can be much smaller and simpler than comparable Intel chips, Mr. Ditzel said.

As a result, the Crusoe chips cost less, can run on low power, and can easily fit into portable machines. By contrast, Intel's chips are speed kings, but they are much larger in size and consume so much power that laptops can't run on batteries for a long time. Intel Tuesday introduced a technology to make laptops run at higher speeds if plugged into a socket or at a lower speed, power-conservation mode while on batteries.

But Mr. Ditzel said his chips would make Intel's technology look "rather rudimentary." On Wednesday, Robert Jecman, vice president of Intel's mobile-computing group, declined to comment on Transmeta's impending launch.

The entry of Transmeta could shake up the PC-chip market, where Intel now has an commanding 82% market share. Intel has begun making chips for the so-called "information-appliance" market, which consists of devices that connect to the Internet but don't necessarily use Windows software. Transmeta's chips are targeted at handhelds and portable computers -- whether they be appliances or actual PCs.

A Family of Chips

Transmeta said its TM5400 chip will run Windows, run at 700 MHz and is designed for lightweight notebook computers. The TM3120 will run the Linux operating system, operate at peak power of 400 MHz and fit into mobile Internet appliances, the company said.

Transmeta said the TM3120 is available now, with the TM5400 scheduled to be in production

by mid-2000.

One of Transmeta's major attractions to notebook-computer and Internet-device makers will be the price of its chips. Transmeta said the TM3120 chip will sell for $89 for the 400 MHz model and $65 for the 333 MHz model. The company sees the chip being used in Internet devices selling from $500 to $999.

The TM5400 chip is expected to sell at $119 for the 500 MHz version and at $329 for the model running at 700 MHz. Notebooks using the chips should sell for between $1,200 and $2,500, and be able to run applications designed for the Windows platform, the company said.

All-Stars Blew Company's Cover

Mr. Ditzel's company has only 200 employees, compared with Intel's tens of thousands. But it has an all-star pedigree of executives, board members, venture capitalists and business partners. To date, Transmeta has raised more than $100 million in multiple rounds of funding, Mr. Ditzel said.

Mr. Ditzel, a former top chip architect at Sun and one of the principal creators of the 1980s chip architecture known as "reduced instruction set computing," tried hard to keep the company secret since forming it with eight other computer gurus in 1995. He operated quietly from a headquarters in Santa Clara, and even had employees put trash into special garbage cans so that sensitive company data couldn't be obtained by the numerous spies who dove into the firm's dumpsters.

But the venture was too big to keep secret. Top names such as Linus Torvalds, creator of the free Linux operating system, joined the company and brought unwanted media attention.

"I think if we didn't have Linus, we could have pulled off the secrecy," said Mr. Ditzel, who referred to Mr. Torvalds as the "world's greatest programmer."

The company's board includes Hugh Barnes, former chief technical officer at Compaq Computer Corp.; Murray Goldman, former executive vice president in charge of Motorola Inc.'s chip group; Pete Thomas of Institutional Venture Partners; Bill Tai, formerly of Walden Group and now at Institutional Venture Partners; and Mr. Ditzel. On Wednesday Mr. Ditzel will name Mark Allen, an operations executive at Nvidia Corp., as president and chief operating officer of Transmeta.

Other key people include Colin Hunter, financial adviser, and James Chapman, former vice president of sales and marketing at Intel's old foe, Cyrix Corp.

Backers include seed investors Walden Group and Institutional Venture Partners. Others include Integrated Capital Partners, Microsoft co-founder Paul Allen's Vulcan Ventures, the Soros Fund, Deutsche Bank, Tudor Investments, Invimed, and Novus Ventures.

Can They Deliver?

With the secrecy out of the way, many industry observers are now asking whether Transmeta can deliver on its promises.

"The big question is performance," said Keith Diefendorff, senior analyst at MicroDesign Resources.

During its presentation, Transmeta unveiled testing results based only on its own benchmarks, which left analysts wondering how the chips would stack up using standard benchmarks other chip developers use.

Analysts also said they haven't yet had the opportunity to examine Transmeta products to see whether the company's claim of significant battery-life improvements are true.

Transmeta also declined to identify current customers, saying only that it expected hardware makers to introduce products over coming months.

Using software to provide operating instructions to a chip -- a process called emulation, where programs are translated into a form the hardware understands -- is an old idea in the industry, Mr. Diefendorff said. What Transmeta appears to have done to distinguish its products is to design a processor from the ground up to speed up the software, he said.

Raising Money Was Tough Early On

Mr. Ditzel said the company started as an idea in 1995. He was one of the founders of RISC computing, which favored the simplification of computer chips. In 1980, he co-wrote a paper dubbed "The Case for RISC" with David Patterson, a computer-science professor at the University of California at Berkeley. Mr. Ditzel later joined Sun and became one of its chief chip architects.

But Mr. Ditzel had become disenchanted with the growing complexity of both RISC chips and Intel's own x86 chips. He consulted eight different computer software and hardware experts and enlisted all of them to join the company. Each brought different skills, such as Mr. Hunter, a computer pioneer who was an expert at translating software.

"We'd meet at my home for the first six months," Mr. Ditzel recalled. "I'd look out from my balcony at my home in Palo Alto and see all of Silicon Valley. We decided we had to give it a

try."

The approach they took was called "very long instruction word," or VLIW, which is very similar to what Intel is working on in its joint venture with Hewlett-Packard Co. But Mr. Ditzel said that he believes his company took a simpler approach than Intel.

Raising the money was tough, Mr. Ditzel said, because funders wanted to steer their money into Internet companies "with five people who would take it public in a year." Mr. Ditzel said he had to constantly raise money every six months to keep the venture afloat.

A couple of early prototypes didn't work, and one chip was scrapped. But Mr. Ditzel said the team kept debugging their work, and found that they had created tools that allow chip flaws to be discovered quickly.

International Business Machines Corp. will manufacture the chips for Transmeta. Besides bringing a well-honed chip-manufacturing operation, IBM also offers the small company an important legal shelter against Intel because it has a patent cross-licensing agreement with Intel. Customers are expected to begin announcing computers with Crusoe chips shortly.

Mr. Ditzel said the family of chips is called Crusoe, after Daniel Defoe's classic "Robinson Crusoe," the story of a man stranded on a desert island. Mr. Ditzel said he liked the word's connotation of "adventure, self-sufficiency, and the idea of someone sitting on an island and getting a lot of work done."

-- Mark Boslet of Dow Jones Newswires contributed to this article.

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EXHIBIT 4

Cahners
MICROPROCESSOR REPORT
Volume 14, Archive 2 www.MPRonline.com February 2000
THE INSIDER'S GUIDE TO MICROPROCESSOR HARDWARE

TRANSMETA BREAKS X86 LOW-POWER BARRIER

VLIW Chips Use Hardware-Assisted x86 Emulation

By Tom R. Halfhill {2/14/00-01}

Like moths drawn to a flame, semiconductor startups seem to find the bright but dangerous glow of the x86 market irresistible. Never mind that companies as resourceful as AMD, Centaur, Cyrix, IBM, National Semiconductor, and Rise have all charred their wings in the fires of competition with Intel. More than 120 million x86 chips were sold in the profitable PC market last year, casting off a warmth that lures newly hatched companies from the darkness.

The latest newcomer to emerge from its cocoon is Transmeta. After nearly five years of unprecedented secrecy, the Santa Clara–based startup finally unveiled its pair of x86-compatible Crusoe processors at a widely covered media event near Silicon Valley last month. The event received the same sort of overhyped coverage the U.S. Air Force might attract by flinging open the gates to Area 51. A large crowd of mainstream and business journalists were dazzled by marketing claims about "revolutionary" microprocessors that are "part hardware, part software" and that rely on something called "code morphing" to achieve x86 compatibility at amazingly low power levels.

What's behind the hype? Transmeta announced a pair of VLIW chips that have special hardware and software for emulating other instruction sets, and they can also dynamically scale their voltage and core frequencies to conserve power. Revolutionary may be an overstatement, but they are definitely different.

A Fresh Approach to the x86

Transmeta could have followed the well-trodden path of designing chips that clone the devilish x86 architecture entirely in hardware, but that's a technically difficult and legally hazardous endeavor. (Ask AMD and Cyrix.) Instead, the company created a new VLIW architecture with a software envelope that translates x86 binaries into native code at run time.

Continued on page 9

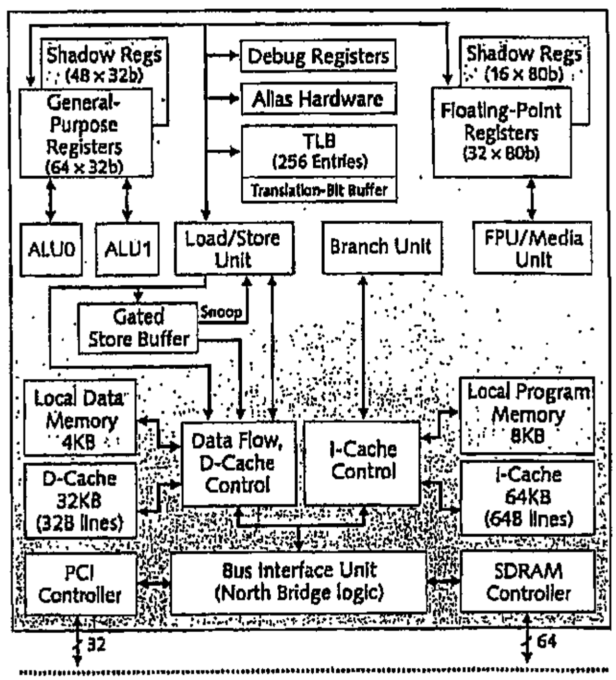

Figure 1. Transmeta's Crusoe TM3120 processor has special features (highlighted in purple) that improve software performance, particularly when translating nonnative code into native VLIW instructions.

TRANSMETA BREAKS x86 LOW-POWER BARRIER

(Continued from Page 1)

While some companies have used the term "emulation" to describe the binary-translation process, Transmeta founder Dave Ditzel shuns that term, preferring to describe his company's method of converting x86 instructions into VLIW instructions as "code morphing" or simply "translation." Sometimes this process is called dynamic binary recompilation. Transmeta's code-morphing software certainly is more advanced than old-fashioned emulators, which slowly convert one type of binary executable into another by translating one instruction at a time. Although Transmeta's code-morphing software begins translating a program that way, it gradually identifies sections of frequently executed code in the nonnative program, dynamically recompiles those sections into optimized native instructions, and then caches the native code for reuse. Those techniques greatly improve performance.

Other modern emulation packages use similar techniques, however. Examples include FWB's SoftWindows for the Macintosh and for Unix, Connectix's Virtual PC for the Mac, FX!32 for Alpha, and Sun's HotSpot, a Java just-in-time (JIT) compiler. For the purposes of this article we will sometimes refer to any process of translating one type of binary executable into another at run time as "emulation," on the grounds that optimizing and caching the translated code are performance-enhancing techniques that do not alter the fundamental character of what's going on.

One thing that sets Transmeta's Crusoe processors apart is special hardware to assist emulation—although this too is not a completely novel approach. In 1992, International Meta Systems (IMS) announced the 3250, a microprocessor designed to emulate the x86, 68K, and 6502 architectures by using customizable microcode, among other techniques (see *MPR 5/6/92-03*, "Microcode Engine Offers Enhanced Emulation"). But the 3250 never reached the market, and IMS went up in smoke.

For reasons that are perhaps more legal than technical, Ditzel says the special hardware in Crusoe chips isn't specifically for x86 emulation. Strictly speaking, this is true. The special features should boost the performance of any nonnative executables that Transmeta targets for translation, as well as the performance of native VLIW software. Transmeta has even demonstrated Crusoe processors running Java programs by translating Java bytecodes into native VLIW code. As we'll explain later, though, it's probably more than just a coincidence that Crusoe chips have 80-bit-wide floating-point registers, the ability to perform partial-register writes, and native support for the same data types and single-instruction multiple-data (SIMD) operations found in Intel's MMX extensions. Those features are eerily reminiscent of the x86 architecture, and they will improve Crusoe's ability to run any x86 code the chips should happen to encounter.

Transmeta's most important accomplishment is combining the concept of dynamic binary recompilation with the inherent efficiency and parallelism of VLIW. The result is a pair of x86-compatible processors unlike any others on the market. Beyond that, Crusoe chips appear to achieve three additional milestones:

- Thanks to a unique hardware/software technology called LongRun, the higher-end version of Crusoe can dynamically vary its voltage and clock frequency by monitoring the changing demands of application programs. The processor can scale its performance and power consumption up or down in small increments to conserve power. This innovative technique should greatly improve battery life in mobile systems.
- Crusoe chips appear to set a new standard for low power consumption among x86-compatible processors. Transmeta claims the typical power consumption of its fastest 700-MHz chip is only 1–2W, which is significantly less than the 14–21W consumed by a 650MHz Mobile Pentium III. These claims haven't been independently verified yet, but if they're remotely accurate, Transmeta can exploit a key vulnerability of the hand-me-down desktop chips that Intel and AMD sell into the mobile market.
- Crusoe processors appear to sacrifice much less performance to emulation than other software translators. According to Ditzel there's actually no translation overhead at all—Crusoe chips are slower than similarly clocked x86 chips merely because Transmeta optimized the cores for low power consumption, not performance. The company says a 700MHz Crusoe is about 70% as fast as a 700MHz Pentium III. If that claim proves accurate, Crusoe's unusual approach to x86 compatibility subtracts less performance than might be expected.

In short, Transmeta doesn't need revolutionary technology or media hype to succeed. Low power consumption and adequate performance should be enough to secure Transmeta a profitable future in the competitive x86 market—if the fledgling company can deliver everything it promises.

Two Chips for Two Markets

Transmeta has announced two versions of Crusoe: the TM3120, which will be available in speed grades of 333, 366, and 400MHz, and the TM5400, which will be available in speed grades ranging from 500 to 700MHz. Both chips are sampling now, and the TM3120 is in production. The TM5400, a later design that improves on the TM3120, is scheduled for production in 2Q00. Prices range from $65 to $89 for the TM3120, and from $119 to $329 for the TM5400.

IBM Microelectronics will manufacture both processors as part of a foundry arrangement that gives Transmeta

valuable patent protection, because IBM has a comprehensive patent cross-licensing agreement with Intel. IBM is packaging the chips in 474-contact BGAs. Because the TM3120 and TM5400 have different bus structures, the TM3120 has about 80 unused pads in this package, but Transmeta says the common pinout makes it easier for customers to design boards that work with either chip. The packages can be soldered onto the motherboard or mounted in a new type of socket from FormFactor/Tyco Electronics. The socket works with BGA and LGA chips and has a lower profile than the soldered MBGA (micro-BGA) packages favored by Intel.

Transmeta designed the two Crusoe chips for quite different markets. The TM3120 is for mobile Internet appliances, while the TM5400 is for Windows-compatible notebook PCs. The latter market is well established, and OEMs should welcome a new x86-compatible CPU that consumes only a few watts. The market for mobile Internet appliances, while nebulous today, is expected to be a fast-growing market in the future.

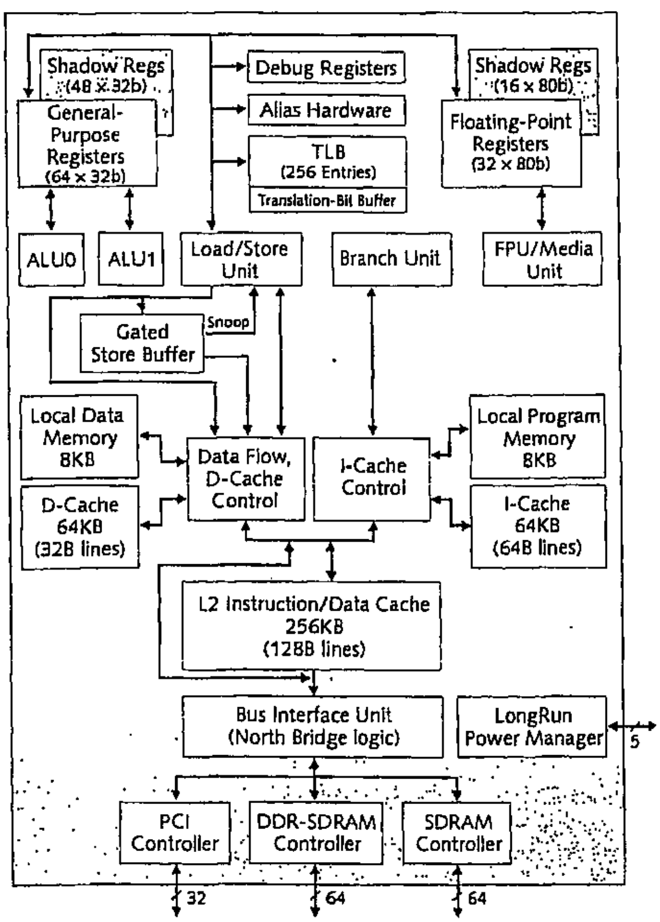

Figure 2. Transmeta's Crusoe TM5400 has some features not found in the lower-end TM3120: an on-chip L2 cache, a DDR-SDRAM controller, LongRun power-management hardware, larger caches, and a slightly different instruction set.

The TM3120, seen in Figure 1 (on page 1), is the lower-end chip. It has 96K of primary cache, divided into a 64K instruction cache and a 32K data cache, both eight-way set-associative. There is no on-chip secondary cache. The TM3120 has an integrated PCI controller, an SDRAM controller, and other components of a traditional north bridge; therefore Transmeta won't have to rely on other companies to provide compatible core logic, and the processor gains the power-consumption and performance efficiencies of an on-chip memory controller. IBM is building the TM3120 in its 0.22-micron copper CMOS-7S process. This process allows up to six metal layers, but the TM3120 uses only five. The chip's die area is $77mm^2$.

The TM5400, seen in Figure 2, is the higher-end model. It has 128K of primary cache, evenly divided into an 8-way set-associative instruction cache and a 16-way set-associative data cache. (The TM5400's data cache has twice the set-associativity of the TM3120's data cache in order to keep each set at 4K, which matches the page size of the x86.) The TM5400 also has a four-way set-associative 256K secondary cache on chip, which should improve performance over the TM3120. Like its fellow Crusoe chip, the TM5400 integrates a PCI controller, an SDRAM controller, and north-bridge functions, but it also supports double-data-rate (DDR) SDRAM on a separate bus. IBM is building the TM5400 in its 0.18-micron copper CMOS-8S process. This process allows up to seven metal layers, but the TM5400 uses only five. The chip's die area is $73mm^2$.

One significant difference between the TM3120 and the TM5400 is that the latter chip has the LongRun voltage/frequency-scaling hardware, which allows the 700MHz TM5400 to consume only a little more power than the 400MHz TM3120. It's likely that all future Crusoe processors will incorporate LongRun.

In most other ways, the two chips are similar. Both are VLIW machines that execute 64- or 128-bit instruction bundles, with each bundle containing two or four 32-bit subinstructions, as shown in Figure 3. Transmeta refers to the VLIW bundles as "molecules" and to the subinstructions as "atoms." If the translation software can't fill all the subinstruction slots in a molecule with useful atoms, it pads the empty slots with NOPs (null operations). By allowing two types of molecules—one with two atoms and one with four atoms—Transmeta ensures that no molecule ever has to carry more than one NOP. This minimizes the space and fetch bandwidth wasted by NOPs, which are the Achilles' heel of traditional VLIW architectures.

Both Crusoe chips have two integer ALUs, a load/store unit, a branch unit, and an FPU/multimedia unit, allowing them to execute up to four VLIW subinstructions per cycle. Their execution pipelines are identical, as shown in Figure 4. Both chips also have 64 general-purpose registers (GPRs) that are 32 bits wide and 32 floating-point r isters (FPRs) that are 80 bits wide. Although the Fi multimedia unit can handle the same data types as Intel's

MMX instructions, Crusoe chips don't have the new 128-bit registers defined by Intel's SSE (Streaming SIMD Extensions). Transmeta says Crusoe could emulate SSE-type instructions and registers, but there's not enough software support for SSE to justify the effort at this time. Crusoe doesn't support AMD's 3DNow! extensions, either.

The architectural features of Crusoe chips are of little importance to software developers, because nobody except Transmeta writes software for the native architecture. To operating systems, development tools, and applications, the chips look like regular x86 processors. Transmeta has no plans to develop native VLIW applications or to encourage others to do so. In fact, Transmeta discourages native software development, because the company wants the freedom to change the architecture from one processor generation to another, or even from one chip to another in the same generation.

Indeed, the TM5400's instruction set has some improvements over that of the earlier TM3120, so their VLIW binaries are not 100% compatible. Future Crusoe processors may introduce completely different instruction sets or architectures. It doesn't matter to users or to software developers, because the only software that runs natively is Transmeta's own code-morphing software, which runs transparently below the operating system.

The first publicly announced Transmeta customer was S3, which is working on a "Web pad" appliance based on a 400MHz TM3120. The prototype has a 10.4-inch color LCD screen, a hard disk drive, and wireless network connectivity. It weighs 2–3 pounds with a rechargeable battery and runs Mobile Linux, a special version of Linux designed by Transmeta. (Interestingly, Transmeta says it hired Linux creator Linus Torvalds primarily for his programming prowess and that his work on Mobile Linux was a relatively minor part of his job.)

S3 plans to introduce the Web pad later this year at a retail price of $500–$1,000, although it could cost less if subsidized by an Internet service provider. S3's chief technology officer, Andy Wolfe, says his engineers chose the Crusoe processor over alternative x86 chips because of its low power consumption, which extends battery life and eliminates the need for a cooling fan. Some embedded RISC chips met the same power and performance requirements, but they aren't x86 compatible, so they can't run the growing number of Web-browser plug-ins that Wolfe considers vital for the product.

LongRun Extends Battery Life

The TM5400's LongRun feature is one of the most innovative technologies introduced by Transmeta. To our knowledge, no other microprocessor can conserve power by scaling its voltage and clock frequency in response to the variable demands of software. Intel's SpeedStep—announced the day before Transmeta's coming-out party—is crude in comparison. It merely steps down the CPU clock and supply voltage when a user unplugs a mobile computer from AC power, and it has only one voltage/frequency step (from 650 or 600MHz to 500MHz).

LongRun can scale the CPU's voltage in as many as 32 steps, though in practice 5–7 steps are sufficient to achieve most of the benefits, according to Transmeta engineers. There are individually controllable, codependent ranges for voltage and frequency. In the current version of the TM5400, voltage can vary from 1.1V to 1.6V, and frequency can vary from 200MHz to 700MHz in increments of 33MHz. Transmeta's software controls the scaling through a five-pin interface that adjusts an off-chip voltage regulator, as seen in Figure 2.

When the LongRun software detects a change in the CPU load, it signals the chip to adjust the voltage and frequency up or down. (It's not exactly clear how LongRun measures CPU loads; even an idle loop can make a CPU seem very busy. This function may be related to x86 emulation, because Transmeta's code-morphing software constantly monitors software execution to control binary recompilation, as explained later in this article.) If the CPU needs to handle a heavier load, LongRun tells the chip to start ramping up its voltage. When the voltage stabilizes at the higher level, the chip scales up its clock frequency.

If the LongRun software determines that the CPU can save power by running more slowly, the chip starts scaling down its frequency. When the phase-lock loop (PLL) locks onto the lower clock rate, LongRun reduces the voltage. By always keeping the clock frequency within the limits required by the voltage, LongRun avoids any clock skewing or other undesirable effects.

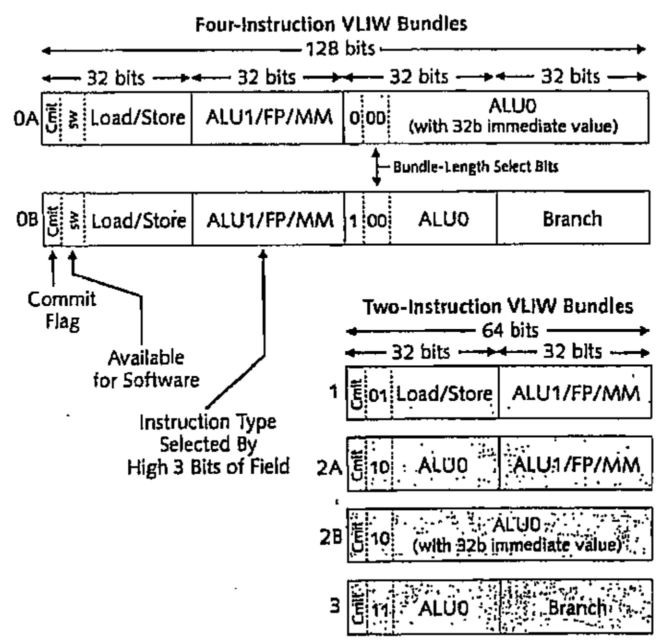

Figure 3. There are six possible types of VLIW bundles. They vary by length and by the arrangement of subinstructions within the bundles.

LongRun never needs more than one frequency step to reach a different target. To scale from 600 to 700MHz, for instance, LongRun doesn't have to take three 33MHz steps. Instead, it raises the voltage to 1.6V in multiple steps, then boosts the frequency to 700MHz in one big jump. This avoids the latencies of resetting the frequency multiple times.

One concern is that LongRun might not react quickly enough to accommodate the fast-changing demands of some programs. When the computer is playing MPEG-compressed video, for example, a transition from a relatively static frame to an action-filled frame might overwhelm a CPU that's comfortably loafing at a low clock speed. MPEG compression works by saving the differences between frames, and the frames are only 1/30 of a second apart. The CPU load would vastly increase after a sudden transition from an Al Gore speech to a car chase.

Not to worry, says Transmeta. The company claims its software can detect a change in the CPU load in about half a microsecond, and LongRun can scale the voltage up or down in less than 20 microseconds per step. The worst-case scenario of a full swing from 1.1V to 1.6V and from 200 to 700MHz takes only 280 microseconds.

Furthermore, Transmeta says, the CPU doesn't stall during the swing, as a mobile Pentium III does during a SpeedStep adjustment. The processor keeps executing instructions, stalling only while the PLL relocks onto the new frequency. That doesn't take longer than 20 microseconds in the worst case, and Transmeta's engineers say they've never observed a relock taking longer than 10 microseconds.

LongRun isn't the only reason that Crusoe processors appear to consume much less power than comparable x86 chips. The TM3120 doesn't have LongRun, yet its power consumption is impressive too. The simplicity of Transmeta's VLIW architecture is evidently a larger factor. Some embedded RISC chips are even more efficient—Intel's second-generation StrongARM, which will ship in 2H00, is expected to consume only 450mW (typical) at 600MHz. But when x86 compatibility matters, Crusoe is the front-runner, and LongRun is a genuine innovation that gives Crusoe an extra edge.

Technology Drives Transmeta's Strategy

Intel and AMD are more vulnerable in the mobile market because their cores are not primarily designed for low power consumption. Typically, Intel and AMD repackage their desktop processors as mobile processors when shrinking process technology and aggressive power management reduce power consumption into the range considered acceptable for notebook PCs. Transmeta's cores are better suited for mobile applications because their relatively simple VLIW architectures are more efficient than the x86 architecture. To counter Transmeta's claimed power-consumption advantage, Intel and AMD would have to introduce new x86 cores specifically designed for low power—a costly undertaking that probably only Intel could justify. VIA's future WinChips might give Crusoe some competition, but we don't know enough about their power consumption to draw any conclusions.

Pursuing mobile PCs instead of the larger desktc market also relieves some pressure on Transmeta. As other companies have discovered, performance is paramount in the desktop segment. An x86 vendor must match or exceed Intel's clock frequencies to maintain profitable selling prices, and Intel has enormous advantages in engineering resources, fabrication technology, and manufacturing capacity. Even a company as large as AMD has trouble keeping up.

Transmeta doesn't rule out introducing future processors aimed at the desktop or even the server markets. Ditzel says there's no inherent penalty for translation, so a future Transmeta processor with code-morphing software could compete with native x86 chips on raw performance. If his claim is true, then Transmeta may indeed have advanced the art of emulation beyond anything seen before.

Traditionally, the ovr head of emulating anotl CPU architecture in software is

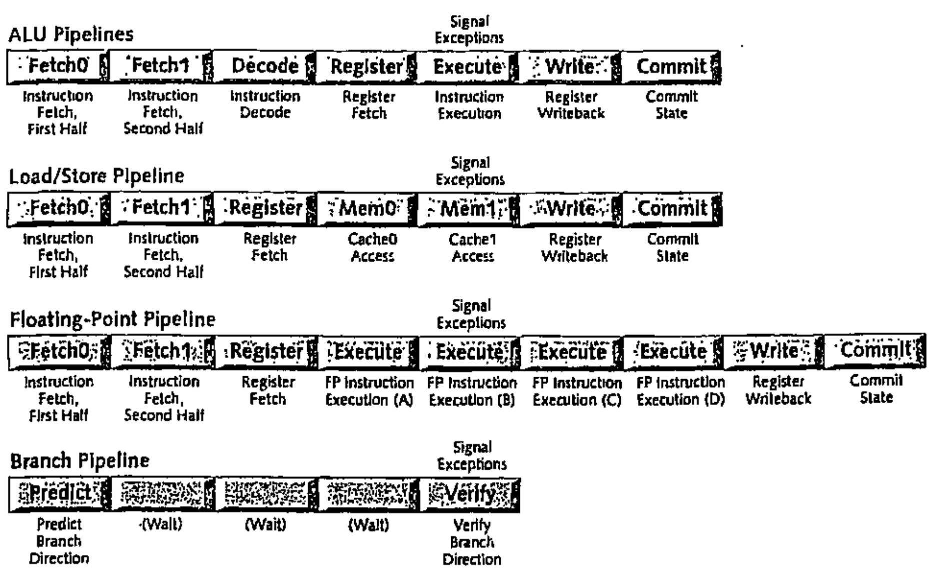

Figure 4. Crusoe processors have shorter pipelines than most x86-compatible processors.

highly variable. In terms of clock cycles, it's generally about 10 to 1. By using such techniques as caching and optimized recompilation, modern emulators can reduce that ratio to 4 to 1 in some cases. Transmeta says its 700MHz TM5400 delivers about the same performance as a 500MHz Pentium III on industry-standard application-level benchmarks, which is significantly better than 4 to 1. S3's Andy Wolfe says a 400MHz TM3120 runs software on Mobile Linux about as fast as a 333 or 400MHz Intel Celeron runs comparable software on Windows 98—although he acknowledges that Linux, not just Transmeta's code-morphing software, is a major factor.

For reasons explained below, Transmeta's performance claims are difficult to verify independently because of the way modern emulators work. The important point is that Transmeta's current processors are better suited to mobile and embedded applications, where power conservation matters more than raw performance.

The keys to a low-power design are minimizing the amount of switching logic and shrinking the die. Transmeta's choice of a VLIW-based architecture makes sense, because VLIW can, theoretically, extract lots of instruction-level parallelism from program code without the complex control logic that burdens superscalar RISC and CISC processors. Crusoe chips are admirably small; see the die photos in Figure 5 and Figure 6. (Transmeta hasn't released transistor counts for either chip.) The inherent efficiency of VLIW has made it the darling of CPU architects, superseding RISC as the design pattern for most new architectures. In recent years, VLIW variants have been announced by Analog Devices, Equator, Fujitsu, Hewlett-Packard, Intel, Philips, StarCore, Sun, and Texas Instruments. All were inspired by the pioneering work of Cydrome, Culler, and especially Multiflow in the 1980s (see *MPR 2/24/94-05*, "VLIW: The Wave of the Future?").

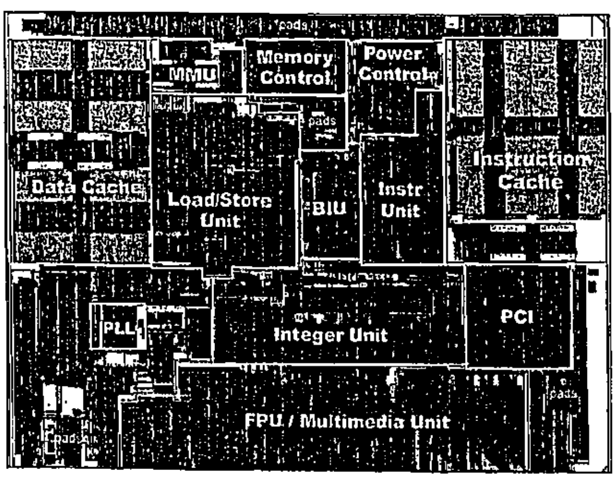

Figure 5. The Crusoe TM3120's die size is 77 mm^2. Note the PCI controller and memory controller; the north bridge is also on chip.

Transmeta's focus on the x86 makes sense, too—at least for Crusoe chips aimed at the PC market, where x86-based Windows software reigns supreme. In the embedded market, the x86 has been trampled by RISC architectures, such as ARM, MIPS, and SuperH. But that's largely because RISC chips are more power-efficient than x86 chips with comparable performance, and also because there's no dominant x86 software base.

Crusoe could alter that picture. The chips appear to be competitive with the performance/power-consumption ratios of many embedded RISC chips. And because they are x86-compatible, they can run Web-browser plug-ins and other software that would require more extensive porting to run on RISC processors. That could be an important advantage for newfangled information appliances like S3's Web pad.

In that regard, Transmeta's strategy is similar to National Semiconductor's. Last year, National announced the x86-compatible Geode SC1400 for the embedded market and also demonstrated a prototype Web pad (see *MPR 8/2/99-03*, "National Unveils 'Appliance On a Chip'"). The SC1400 is more highly integrated than Crusoe. It incorporates not only the north-bridge logic, PCI controller, and SDRAM controller, like Crusoe, but also a VGA-graphics accelerator, an MPEG audio/video processor, a video-overlay processor with NTSC and PAL outputs, an IDE interface, a three-port USB interface, and numerous UARTs and general-purpose I/O ports.

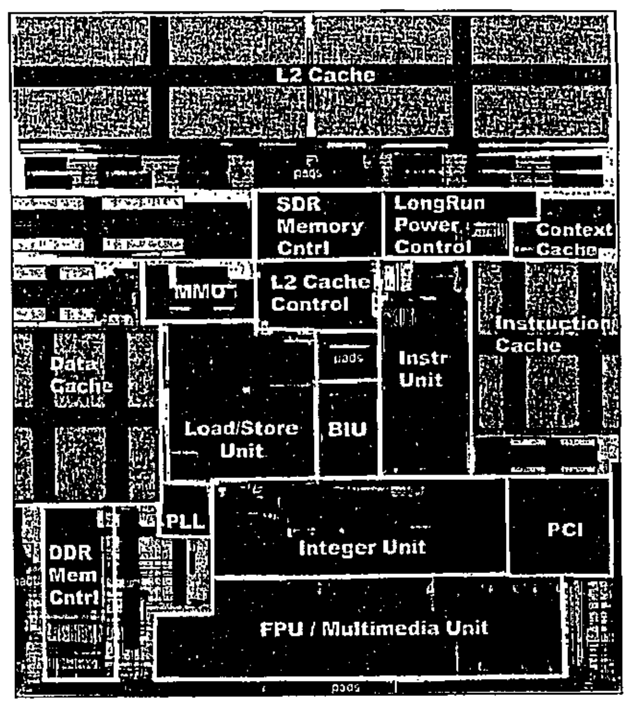

Figure 6. The Crusoe TM5400's die size is 73 mm^2. In addition to a PCI controller, memory controller, and north bridge, it also has 256K of on-chip L2 cache.

Transmeta's TM3120 should be faster than the SC1400, which is built around an old 486-class Cyrix core that runs at 233–266MHz and delivers about the same performance as a fast Pentium. Power-consumption comparisons are difficult because National hasn't publicly released those figures for the SC1400, and also because Crusoe processors need additional logic to match the higher integration of the SC1400. But Crusoe has one big advantage: a deep-sleep mode that consumes less than 20mW. The SC1400 conspicuously lacks a deep-sleep mode. National needs to upgrade its Geode chips to stay competitive with upstarts like Transmeta.

Decoding x86 Binaries in Software

Transmeta's claim that Crusoe is "part hardware, part software" isn't merely hype. The code-morphing software performs the x86-instruction decoding that all other x86 processors implement in hardware. The "decoding," in this case, actually involves translating x86 instructions into native VLIW instructions. Although competitors will probably attack this unusual approach to x86 compatibility, there's no technical reason that it can't it work as reliably as traditional approaches.

Current Intel and AMD x86 processors convert x86 instructions into RISC-like micro-ops that are simpler and easier to handle in a superscalar microarchitecture. (In contrast, Cyrix and Centaur cores execute x86 instructions directly.) The micro-op translation adds at least one pipeline stage and requires the decoder to call a microcode routine to translate some of the most complex x86 instructions. Implementing the equivalent of that front-end translation in software saves Transmeta a great deal of control logic and simplifies the design of its chips. It also allows Transmeta to patch some bugs in software. (The engineers fixed a timing problem in the TM5400 in this manner.) Some x86 chips, such as Pentium III, allow some patches to microcode, but these patches are very limited in comparison.

Transmeta's software translation is a little more like the Motorola 68K emulation built into PowerPC-based Macs since 1994. The Mac OS translates ("decodes") 68K instructions into PowerPC native instructions at run time, allowing Power Macs to transparently run older Mac software. This translation works extremely well, and 68K programs actually run faster under emulation on almost all Power Macs than they do on the fastest 68K Macs (thanks to higher clock frequencies). FWB's SoftWindows and Connectix's Virtual PC for the Mac translate x86 binaries into PowerPC instructions, and those translators work well too. Software emulation is a proven concept, dating back at least as far as 1964, when IBM's new System/360 provided emulation for IBM's older 1401 computers.

What's new about Transmeta's approach is that translation isn't merely an alternative to native execution—it's the whole strategy. Crusoe does for microprocessors what Java does for software: it interposes an abstraction layer that hides internal details from the outside world. Just as a Java programmer can write code without needing any knowledge about the underlying operating system or CPU, x86 programmers can continue writing software without needing any knowledge about a Crusoe system's VLIW architecture or code-morphing software.

x86-Flavored VLIW

Crusoe processors have several features that assist the code-morphing software, and some of the features are unmistakably x86-specific. One example is the register files, which have 160 physical registers. These include 64 GPRs with 48 shadow registers and 32 FPRs with 16 shadow registers. The GPRs are 32 bits wide and support partial-register writes, just like real x86 registers. The FPRs are 80 bits wide, so they can directly support x86 extended-precision floating-point operations. (Compaq's FX!32 emulator for Alpha requires extra steps to support 80-bit math in x86 programs because Alpha's FPRs, like those in most RISC processors, are only 64 bits wide.)

The translation software uses the shadow registers to checkpoint the speculative state of the CPU while programs alter the contents of the working registers. This allows Crusoe to execute instructions speculatively and out of order. If an exception occurs, the processor can roll execution back to the most recently committed state of the machine by copying the contents of the shadow registers into the working registers. This also preserves the prec exception model of the x86 (such as it is).

VLIW bundles can include a one-bit "commit" flag that tells the processor to commit the working state of the GPRs and FPRs by copying their contents to the shadow registers. Typically, the translation software commits the results of a block of code before proceeding to the next block of code. In no case will the processor commit results until it has resolved all conditions that might trigger an exception.

One example of a condition that might cause an exception is a sequence of instructions that contains a memory load or store operation. The translation software can reorder loads and stores, moving them higher in the instruction stream to hide memory latencies. Crusoe processors have special alias hardware (see Figures 1 and 2) that watches for subsequent instructions that access memory locations whose data is already loaded in a register. If an instruction tries to access one of those memory locations, the alias hardware raises an exception, and the processor rolls back to the last committed state. The translator then continues forward from that point without using such aggressive optimizations.

The translator can also eliminate redundant loads. If no instructions alter the contents of a memory location between loads, the translator detects the redundancy, skips the unnecessary loads, and uses the data from the first lo· This can happen frequently in architectures with as few reg isters as the x86.

Another mechanism that protects the state of the machine is a gated store buffer, also shown in Figures 1 and 2. The processor temporarily holds the results of all store operations in this 32-entry buffer until an instruction commits the next block of results. At that point, the gate opens and the processor writes the results back to memory.

To solve one thorny problem that rankles x86 architects—self-modifying code—the MMU has a special translation-bit buffer in the TLB. When the translator converts a block of nonnative code into native instructions, it write-protects the memory containing the nonnative code by setting a bit in the translation buffer. If a program tries to overwrite the protected memory, the processor can invalidate the translated code, allow the program to change the original code in memory, and then retranslate the modified code.

Crusoe processors also have special caches, independent of the primary instruction and data caches, to hold critical pieces of the translation software's VLIW code and data structures in fast on-chip SRAM. The TM5400 has 8K of local program memory and 8K of local data memory; the TM3120 has 8K of local program memory and 4K of local data memory. The translation software manages these caches directly, so they're not flushed by misses on the regular primary caches.

Parlez-Vous x86?

In other respects, Transmeta uses techniques similar to those in other modern emulators and JIT compilers. The translator dynamically analyzes the run-time behavior of a program, interprets code that the program executes infrequently, recompiles and caches code that the program executes often, and applies common compiler optimizations whenever practical.

When a Crusoe system boots, it immediately reserves a 16M block of main memory, though Transmeta says 8M is acceptable for systems with less RAM. Next, the translator loads from ROM into the reserved memory, occupying about 512K. The rest of the 16M block is set aside as a translation cache, where the translator stores recompiled code for later use. Enlarging this cache beyond 16M contributes little to performance with the kind of software that users tend to run on notebook computers and information appliances, according to Transmeta.

The reserved memory is invisible to the BIOS, the operating system, and the application programs. From the user's point of view, that memory never existed—so a system with 64M of RAM would appear to have only 48M. OEMs determine the size of this memory block when they configure a system at the factory, and normally it's immutable. Some emulators, such as SoftWindows, allow users to change the size of the translation cache to tweak performance. But those emulators run on top of the host operating system, not beneath it as Transmeta's does.

In practice, Transmeta's code-morphing software works much like a Java JIT compiler, and especially like Sun's HotSpot JIT compiler. The translator starts out conservatively, interpreting x86 instructions one at a time without necessarily storing the converted code in the translation cache. There's nothing to gain by caching a program's initialization routine, for instance, because that code executes only once. (An exception might be a large initialization loop that could benefit from caching.) Straight interpretation requires at least 12 clock cycles per x86 instruction.

As the x86 program continues to run, the translator monitors the program's behavior, noting which code is frequently executed. In effect, the translator performs the same analysis as the code profilers used by programmers to identify critical sections in their programs—except the translator does it at run time, gathering information from real users, based on their actual working patterns.

When the translator identifies a frequently executed section of code, it schedules that code for compilation and perhaps for optimization. There are several degrees of possible optimization. Like Sun's HotSpot, the translator estimates how much time it needs to optimize the code and balances that time against the execution time it's likely to save. If the equation makes sense, the translator recompiles the x86 code into VLIW code and stores it in the translation cache. One difference between Transmeta's translator and Sun's HotSpot is that Transmeta can optimize one or more basic blocks of code within subroutines, whereas HotSpot optimizes only whole subroutines (Java methods).

Many of the possible compiler optimizations the translator applies are familiar: loop unrolling, common subexpression elimination, loop-invariant code removal, and so on. Some are x86-specific: the translator can skip instructions that redundantly set x86 condition codes. And some are VLIW-specific: the translator can combine multiple x86 basic blocks into a single VLIW basic block by removing unnecessary branches.

The Devil in the Details

Some code expansion is inevitable when converting CISC binaries into VLIW. The code can expand in two ways: by increasing the number of instructions required to do the same work and by translating the compact x86 instructions into longer VLIW equivalents.

Transmeta's technical white paper on compiler optimization shows an example of 20 x86 instructions collapsing into 10 VLIW instructions. But the 10 VLIW instructions are really VLIW bundles (molecules) that each contain two or four RISC-like subinstructions (atoms). Actually, the translator needs 23 VLIW subinstructions to do the work of these 20 x86 instructions.

Moreover, the example doesn't show that some VLIW bundles contain NOPs wherever the translator couldn't fill slots with useful subinstructions. After restoring the missing NOPs, the translated VLIW code contains a total of

32 subinstructions—50% more than the original x86 code, as shown in Figure 7.

The actual code expansion is worse than that, because subinstructions are always 32 bits long. In the x86 architecture, instructions can vary in length from 8 to 120 bits, and the average length is usually estimated at 16–24 bits. So converting x86 code into VLIW may expand the code 33–100%, even if the instruction ratio is the same. If the white-paper example is typical, add another 50% for the extra subinstructions and NOPs required to do the same work as the x86 code.

Transmeta says the code expansion seems less drastic if the subinstructions are compared to the RISC-like micro-ops that Intel and AMD processors use internally, after the decoders break down x86 instructions into their component operations. This is true, because most of the time, x86 instructions fracture into multiple micro-ops, just as they translate into multiple VLIW subinstructions. That's a fair comparison for the purpose of explaining instruction execution, but it doesn't address the important issues of code expansion. The Intel and AMD micro-ops exist only inside the processor's pipelines; they don't occupy space in memory and caches, and they don't consume I/O bandwidth. In contrast, Transmeta's VLIW subinstructions take up space in main memory (in the translation cache) and in the instruction caches, and the processor has to fetch the subinstructions over the I/O bus, even if they're do-nothing NOPs.

The degree of code expansion caused by translation is not a serious flaw, but it does reduce the effective sizes of the caches in comparison with those of other x86 processors. A 64K instruction cache in a Crusoe chip isn't quite as large as it seems, and neither is the 16M translation cache. If code expansion causes the processor to flush the translation cache more often to make room for newly recompiled code, it's more difficult to amortize the clock cycles spent on recompilation and optimization. This depends on software-usage patterns—switching among multiple applications is less efficient than using one application at a time. Of course, this affects the caches of all CPUs, but it's even more true for Crusoe.

Enlarging the translation cache is one solution, but this cache is already pretty large. Subtracting 16M of RAM from main memory is acceptable for notebook PCs with at least 64M, but it could be troublesome for low-end information appliances with less memory. Paging some of the recompiled code to disk is another possibility, but losing clock cycles to a page fault might be worse than recompiling the x86 code again. Fortunately, RAM is getting cheaper all the time. On balance, users will probably consider the "lost" RAM a worthwhile tradeoff for additional battery life. Still, it demonstrates once more that there's no such thing as a free lunch. Transmeta's technology doesn rewrite the rules that all CPUs must obey.

Transmeta also faces some of the criticism aimed at other VLIW architectures, particularly with regard to its code-morphing software. The performance of VLIW processors depends heavily on the scheduling efficiency of their compilers, because they don't have the dynamic reordering hardware found in superscalar RISC processors. The compiler is responsible for scheduling instructions.

When they designed IA-64, Intel and Hewlett-Packard started with the back end of Multiflow's VLIW compiler, and they have have been refining it for five years. Transmeta started from scratch, pr sumably without a prov. back end. Moreover, an

```
  movl %ecx,$0x3
  jmp lbl1
lbl1:
  movl %edx,0x2fc(%ebp)
  movl %eax,0x304(%ebp)
  movl %esi,$0x0
  cmpl %edx,%eax
  movl 0x40(%esp,1),$0x0
  jle skip1
  movl %esi,$0x1
skip1:
  movl 0x6c(%esp,1),%esi
  cmpl %edx,%eax
  movl %eax,$0x1
  jl skip2
  xorl %eax,%eax
skip2:
  movl %esi,0x308(%ebp)
  movl %edi,0x300(%ebp)
  movl 0x7c(%esp,1),%eax
  cmpl %esi,%edi
  movl %eax,$0x0
  jnl exit1
exit2:
```

20 original x86 instructions:
= 10 VLIW bundles ("molecules")
= 23 useful instructions ("atoms")
= 32 total instructions (including NOPs)

Translator can convert multiple x86 basic blocks into a single VLIW code block

CMIT flag commits the results of the previous block of instructions (not shown)

addi %r39,%ebp,0x2fc,cmit;	NOP;		
addi %r38,%ebp,0x304;	NOP;		
ld %edx,[%r39];	add %r27,%r38,4;	add %r26,%r38,-4;	NOP;
ld %r31,[%r38];	add %r35,0,1;	add %r36,%esp,0x40;	NOP;
ldp %esi,[%r27];	add %r33,%esp,0x6c;	sub.c %null,%edx,%r31;	NOP;
ldp %edi,[%r26];	sel#le %r32,0,%r35;	[illegible]	[illegible]
stam 0,[%r36];	sel#l %r24,%r35,0;	add %r25,%esp,0x7c;	NOP;
stam %r32,[%r33];	add %ecx,0,3;	sub.c %null,%esi,%edi;	NOP;
st %r24,[%r25];	or %eax,0,0;	brcc#lt,<exit2>;	NOP;
br <exit1>;	NOP;	[illegible]	[illegible]

Figure 7. This example, adapted from a Transmeta white paper, shows how the translation software recompiles x86 code into native VLIW code.

IA-64 compiler starts with source code and works statically—a programmer can let the compiler churn overnight, if necessary, to extract the most parallelism. Transmeta's VLIW compiler must translate and optimize an x86 binary file while the program is running. The x86 code has already been compiled once, and it may contain optimizations for specific x86 microarchitectures that have nothing to do with Crusoe's microarchitecture.

One factor in Transmeta's favor is that the translator monitors actual usage patterns at run time—dynamic compilers get better feedback than static compilers. Some other software emulators and Java JIT compilers use these same techniques to great effect, so Transmeta hasn't wandered into unexplored territory. But it's worth noting that the quality of Transmeta's run-time translation will greatly influence the x86 compatibility and performance of Crusoe processors. And users will have to be satisfied with Transmeta's translation software, because it will be available only from Transmeta.

Waiting for Real-World Results

It's difficult to judge Transmeta's accomplishments, because after stripping away the hype, many unconfirmed claims remain. At this writing, there are no independent test results of Crusoe's compatibility, performance, software stability, or power consumption. Indeed, such results will be hard to come by, because the very nature of Crusoe's technology defies conventional benchmarking.

Consider the problem of measuring performance. Benchmark programs that rely too heavily on repetitive loops will overestimate the speed of Crusoe's x86 execution, because the translator will quickly recognize the program's behavior, recompile the loops with optimizations, and execute native code out of the translation cache. The results will be accurate only for users who perform the same small set of repetitive tasks all day. (OK, there are some of you out there.)

Conversely, benchmark programs, such as Winstone, that drive real applications with automated scripts may underestimate Crusoe's performance. The scripts run through a series of tasks and switch among applications at much higher speeds than any real user would, so the translator rarely gets a chance to amortize the cost of compiling and optimizing the code.

Battery-life tests have similar flaws. Unless they mirror real-world usage very closely, they won't yield results that average users can expect from Crusoe-based systems. New benchmark suites must be written to take all these factors into account, as Transmeta pointed out during its public announcement.

We're not too worried about the accuracy of Crusoe's x86 emulation. There are companies that do nothing but test for x86 compatibility, so any bugs should be discovered and fixed early. Also, emulation isn't the experimental technology it used to be. Java JIT compilers and Windows emulators have significantly advanced the art in recent years. A little searching on the Web will turn up dozens of emulators for all kinds of platforms, including emulators for some otherwise-dead machines such as the Apple II, Atari 2600, and Commodore 64. If Transmeta had built an x86 processor in the currently fashionable manner—that is, with hardware decoders that convert x86 instructions into native micro-ops—the designers would have written similar translation code, anyway, except they would have written it in Verilog instead of in C or assembly language. Even if Transmeta's code morphing does have some glitches, they're easily patched in software.

One cause for worry is Transmeta's pricing strategy, which appears to bet heavily that Crusoe-based notebook PCs will deliver enough additional battery life to offset a price/performance gap relative to Intel's mobile processors. Currently, a top-of-the-line 650MHz mobile Pentium III costs $637—almost twice as much as the 700MHz TM5400, which costs $329. But direct comparisons are invalid, because neither chip is as fast as its clock speeds imply. With SpeedStep, the 650MHz mobile Pentium III actually runs at only 500MHz on battery power. If we accept Transmeta's claim that the 700MHz TM5400 is as fast as Pentium III at 500MHz, then Crusoe has a worse price/performance ratio. A 500MHz mobile Pentium III without SpeedStep currently costs only $294, about 10% less than the 700MHz TM5400. The 650MHz Pentium III with SpeedStep costs a lot more, but it delivers at least 30% more performance on AC power than the TM5400. These price/performance ratios are likely to change in Intel's favor as time goes by, because Intel will probably cut prices once or twice before Transmeta ships the TM5400 in 2Q00.

Apparently, Transmeta is betting that Crusoe will deliver enough extra battery life to offset the price/performance disadvantage and the user's loss of 16M of system memory (for the translation cache). Transmeta promises to make "all-day computing" a reality. Even if the TM5400 consumes an order of magnitude less power than Pentium III, users won't get an order of magnitude more battery life, because the CPU in a notebook PC doesn't consume 100% of the system's power. Estimates of the CPU's share range from 20% to 75%, with the rest consumed by the LCD screen, disk drive, and other

Price & Availability

Transmeta's Crusoe TM3120 is in production now and will be available at 333, 366, and 400MHz. The Crusoe TM5400 is sampling now and is scheduled for production in 2Q00; it will be available at speed grades ranging from 500 to 700MHz. Prices range from $65 to $89 for the TM3120 chips, and from $119 to $329 for the TM5400 chips. For more information, go to *www.transmeta.com*.

components. (When making these comparisons, remember that Crusoe integrates a north bridge, whereas Intel and AMD processors require extra chips for those functions.) We feel confident that a Crusoe-based notebook PC will run longer on battery power, but if it's only a couple of hours longer, it might not be enough to make Transmeta's pricing strategy work.

But then, competing against Intel is always a risky gambit. Previous attempts to find chinks in Intel's armor—such as Rise's low-power processors and Centaur's simplified WinChips—have proved time and again that Intel is a formidable foe. In the embedded market, Crusoe faces similar tough competition against RISC chips, but x86 compatibility is a major differentiation that will win some customers for that reason alone.

As we learn more about Transmeta's technology and get samples of the chips for hands-on testing, we'll follow up with more detailed analysis. Until then, if Transmeta can fulfill all its promises, we think Crusoe chips will find profitable niches in the PC-notebook and embedded markets. ◇

EXHIBIT 5

Cahners
MICROPROCESSOR REPORT
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TOP PC VENDORS ADOPT CRUSOE

Transmeta Reveals Roadmap; New TM5600 Has 512K L2 Cache

By Tom R. Halfhill {7/10/00-02}

Four top-tier vendors at PC Expo announced their intention to make notebook computers based on Transmeta's Crusoe processors. Some of these systems will use a new version of Crusoe that has twice as much on-chip L2 cache. Transmeta has also revealed a two-year roadmap of processors with higher clock speeds, greater integration, lower power consumption, and new VLIW cores, as Figure 1 shows.

The four PC vendors throwing their weight behind Transmeta's unusual x86-compatible processors (see *MPR 2/14/00*, "Transmeta Breaks x86 Low-Power Barrier") are Fujitsu, Hitachi, IBM, and NEC. All the vendors plan to introduce notebooks in the ultralight class, ranging in weight from 2.8 to 3.5 pounds, with TFT screens ranging in size from 10.4 to 12.1 inches. The notebooks are scheduled to ship this fall.

Crusoe processors are well suited for lightweight notebooks, because their low power consumption eliminates the need for cooling fans and large heat sinks. Furthermore, ultralight notebooks don't compete in the same performance class as larger, heavier laptops, where Intel's mobile processors have a speed advantage.

Some of the new notebooks will use the Crusoe TM5600, which has 512K of on-chip L2 cache—twice as much as the TM5400 announced in February. In other respects, the TM5600 is identical to the TM5400. It will be manufactured by Transmeta's foundry partner, IBM Microelectronics, in a 0.18-micron copper process and packaged in a 474-pin ceramic BGA. Doubling the L2 cache increased the die size to $88mm^2$, which is 20% larger than the TM5400's die ($73mm^2$).

According to Transmeta, the TM5600 is 5–15% faster than the TM5400 and consumes 2–17% less power. Although doubling the size of the L2 cache and enlarging the die would normally increase power consumption, Transmeta says the TM5600 actually uses less power when running typical Windows software, because it makes fewer accesses to main memory over the 3.3V I/O bus.

However, Transmeta still has not released any results of common industry benchmark tests, such as Ziff-Davis

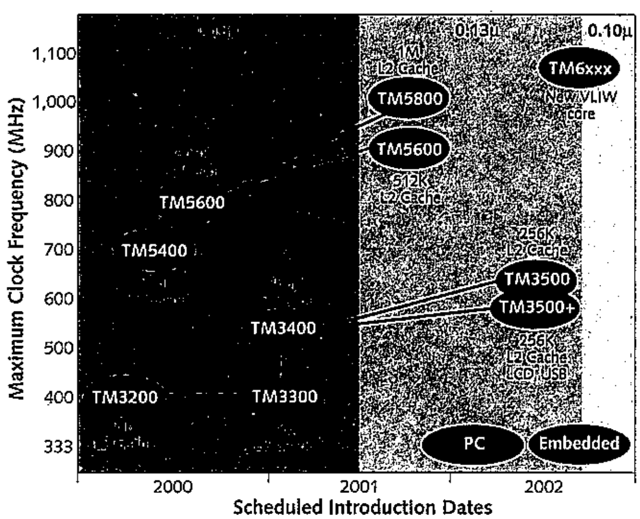


Figure 1. Transmeta's two-year roadmap calls for several new chips based on the existing TM3200 and TM5400 CPU cores, followed by an entirely new core in 2002.

Media's Winstone. Transmeta claims—with some credibility—that existing benchmark programs are misled by the unusual caching and dynamic-recompilation behavior of Crusoe's code-morphing (x86 emulation) software. According to Transmeta's estimates, a TM5400 Crusoe running at 700MHz delivers about the same raw performance as an Intel Pentium III at 500MHz.

Surprising Power Measurements

To back up its claims that Crusoe processors typically consume only 500mW to 1.5W—including the integrated north-bridge controller—Transmeta showed MDR a test system that graphically displays a constant measurement of minimum, maximum, and average power consumption. We experimented with several Windows applications, including Microsoft Word, Internet Explorer, an MP3 audio player, and a DVD movie player. As Figure 2 shows, average power consumption is indeed in the range promised by Transmeta and rarely spikes above 6W. And the test system revealed startling differences in power consumption among applications. For example, merely selecting a paragraph of text in Word briefly gobbled more power than decoding the MPEG-2 stream of a DVD movie.

Faster Crusoe processors are coming next year, according to Transmeta's roadmap. In 2H01, Transmeta will migrate its cores to IBM's 0.13-micron copper process, which offers the option of silicon-on-insulator (SOI) technology (see *MPR 5/1/00-01*, "IBM Paving the Way to 0.10 Micron"). The process shrink will reduce core voltage to 1.2V and boost clock speeds about 25%, even if Transmeta doesn't use SOI. The TM5600 would move into the 700–900MHz frequency range at this geometry.

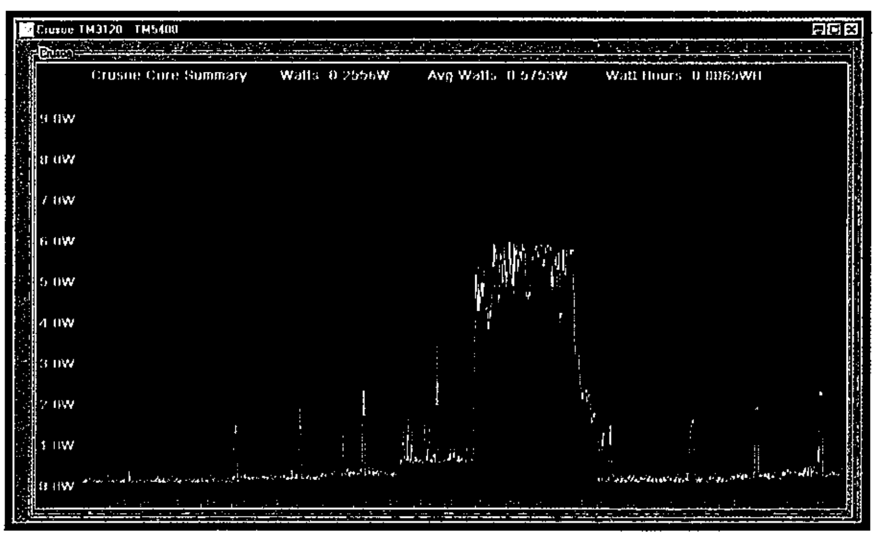


Figure 2. Transmeta's instrumented test system continuously plots power consumption while other software is running. This trace plots the playback of a DVD movie, with regularly spaced spikes marking the decompression and display of each video frame. The large but brief power surge was caused by launching another Windows application.

To take further advantage of the 0.13-micron process, Transmeta plans to introduce another new processor, the Crusoe TM5800, which will have 1M of on-chip L2 cache. It will use the same core as the TM5600 and TM5400 and retain the 474-pin CBGA package.

In 2002, Transmeta plans to revamp its Crusoe line with an entirely new CPU core based on an enhanced VLIW architecture. This core will have a faster FPU and will target a 0.13- or 0.10-micron process. Transmeta expects this unnamed chip (probably TM6xxx) to have twice the performance of existing Crusoe processors while reducing typical power consumption below 500mW.

The code-morphing software will also get an overhaul. Because that software translates x86 instructions into native VLIW instructions on the fly, Transmeta has virtually unlimited freedom to change the inner workings of the CPU core without breaking compatibility with operating systems and applications.

Equally Aggressive Embedded Roadmap

Transmeta's roadmap calls for similar improvements to the company's line of Crusoe processors for Mobile Linux information appliances. The current product is the TM3200, formerly known as the TM3120 (renamed because of a trademark conflict).

Next year, Transmeta plans to introduce two new chips, the TM3300 and TM3400. Both will come in smaller packages (360-pin CBGAs instead of 474-pin CBGAs), achieved by eliminating the unused pads reserved for the DDR-SDRAM interface on TM5xxx-series chips, but they will retain their SDR-SDRAM interfaces. The downsized package will allow Transmeta to sell the TM3300 for less than $50. The TM3400 will be the higher-end model, adding a 256K on-chip L2 cache and LongRun power manager.

In 2002, Transmeta plans to introduce the TM3500, which migrates the existing core to a 0.13-micron process. That will reduce the core voltage to 1.2V and boost the clock frequency to 600MHz. There will also be a more integrated version of the TM3500 that has 256K of on-chip L2 cache, LongRun power management, an LCD controller, a USB interface, and a PCI interface. Those additions will bump the pin count back up to 474 but provide system vendors with a more complete system solution. Table 1 summarizes the features of Transmeta's current and future chips.

Less than six months after its much-hyped public debut, Transmeta has gained the crucial support of some

Feature	TM5400	TM5600	TM5800	TM6xxx	TM3200	TM3300	TM3400	TM3500
CPU Core	5400	5400	5400	6xxx	3200	3200	3200	3200
Core Freq*	500–700MHz	500–800MHz	700MHz–1GHz	>1GHz	333–400MHz	333–400MHz	400–533MHz	400–600MHz
L1 Cache (I/D)	64K/64K	64K/64K	64K/64K	n/a	64K/32K	64K/64K	64K/64K	64K/64K
L2 Cache	256K	512K	1M	n/a	None	None	256K	256K
LongRun?	Yes	Yes	Yes	Yes	No	No	Yes	Yes
SDRAM Ctrl?	SDR+DDR	SDR+DDR	SDR+DDR	n/a	SDR	SDR	SDR	SDR
LCD Ctrl?	No	No	No	n/a	No	No	No	Yes
USB Ctrl?	No	No	No	n/a	No	No	No	Yes
PCI Ctrl?	Yes	Yes	Yes	n/a	Yes	Yes	Yes	Yes
IC Process	0.18µ 5LM	0.18µ 5LM	0.13µ	0.10–0.13µ	0.18µ 5LM	0.18µ 5LM	0.18µ 5LM	0.13µ
Core Voltage	1.6V	1.6V	1.2V	1.2V	1.5V	1.5V	1.5V	1.2V
Die Size	73mm²	88mm²	n/a	n/a	77mm²	77mm²	n/a	n/a
Package	CBGA-474	CBGA-474	CBGA-474	n/a	CBGA-474	CBGA-360	CBGA-360	CBGA-474
Power (typ)	<1.5W	<1.5W	<1W	<500mW	<1.5W	<1.5W	<1.5W	<1W
Price (1K)	$119–$329	n/a	n/a	n/a	$65–$89	<$50	n/a	n/a
Availability	Now	Aug-00	2H01	2002	Now	1Q01	1Q01	2002

Table 1. Transmeta has aggressive plans to expand its Crusoe line over the next two years while taking advantage of IBM's latest semiconductor process. (*In this table, "core frequency" refers to the maximum clock-frequency ratings of individual Crusoe processors, not to the range of frequencies supported by LongRun power management. n/a = information not available.)

top-tier PC vendors and major financial backers. In addition to the PC vendors that announced Crusoe-based notebooks at PC Expo, Gateway has committed to using a Crusoe chip in a Linux-compatible information appliance designed for AOL (see *MPR 6/5/00-04*, "Transmeta Lands Gateway-AOL IA"), and several high-profile investors have kicked in $88 million of funding (see *MPR 5/1/00-06*, "Transmeta Lands $88M").

Although Transmeta's performance and power-consumption claims haven't been independently verified, this situation is clearly not hurting the company's ability to attract key customers and investors. And Transmeta's early success is exerting pressure on Intel to come up with a comparable line of low-power processors.

Telling Watt's Right From Wrong

No doubt in response to Transmeta's challenge, Intel says its latest mobile PC processors come close to matching the average power consumption of the TM5400. On June 19, Intel announced five mobile Pentium III and Celeron processors and claimed their average power consumption to be 0.8–1.6W for the 500/600MHz Pentium III and 1.6–2.8W for the 600/750MHz Pentium III (see *MPR 7/3/00-02*, "Intel Strikes Back at Transmeta").

Those numbers are far below Intel's own thermal design power (TDP) specifications, which represent worst-case design points for engineers who want to ensure that their systems won't overheat. The disparity between Intel's average-power estimates and the TDP specifications provoked a quick reaction from Transmeta. The company accused Intel of manipulating the average-power figures by basing them on tests with Ziff-Davis Media's BatteryMark program, which typically spends 80% of its time in idle states.

Sorting out these claims and counterclaims isn't easy. Intel's TDP specification is 9.5W for the 500/600MHz mobile Pentium III and 15.8W for the 600/750MHz mobile Pentium III. However, those numbers don't include a north-bridge controller, which is integrated on Crusoe chips and included in their power ratings. Intel does offer mobile

Feature	Transmeta Crusoe TM5400	Transmeta Crusoe TM5600	Intel Mobile Pentium III	Intel Mobile Pentium III
CPU Core	5400	5400	Coppermine	Coppermine
Freq Range*	200–700MHz	200–800MHz	600/750MHz	500/600MHz
L1 Cache (I/D)	64K/64K	64K/64K	16K/16K	16K/16K
L2 Cache	256K On-Chip	512K On-Chip	256K On-Chip	256K On-Chip
North Bridge	Yes	Yes	No	No
SDRAM Ctrl	SDR+DDR	SDR+DDR	No	No
PCI Ctrl?	Yes	Yes	No	No
MMX?	Yes†	Yes†	Yes	Yes
SSE?	No	No	Yes	Yes
IC Process	0.18µ 5LM	0.18µ 5LM	0.18µ 6LM	0.18µ 6LM
Metal Layers	Copper	Copper	Aluminum	Aluminum
Core Voltage	1.1–1.65V	1.1–1.7V	1.35/1.6V	1.1/1.35V
Die Size	73mm²	88mm²	106mm²	106mm²
Power Modes	LongRun	LongRun	SpeedStep	SpeedStep
Power (typ)	0.5–1.5W	0.5–1.5W	1.6–2.8W	0.8–1.6W
Power (max)	~6W	~6W	13.9/20W	12.2/16.6W
Price (1K)	$329	n/a	$562	$316
Availability	Now	Aug-00	Now	Now

Table 2. Transmeta's Crusoe processors have an advantage in power consumption, whereas Intel's mobile Pentium III processors have an advantage in performance: Transmeta says a 700MHz TM5400 is about as fast as a 500MHz Pentium III. (*In this table, "frequency range" refers to the variable clock rates of an individual chip in its different operating modes. The TM5400 and TM5600 can vary their frequencies within these ranges in increments of 33MHz, while the mobile Pentium III chips are limited to the two frequencies shown. †Not including north bridge. n/a = information not available.)

Price & Availability

Transmeta will begin shipping production volumes of the Crusoe TM5600 with 512K L2 cache in August. The price has yet to be announced. The TM5400 and TM3200 are shipping now. TM5400 prices range from $119 at 500MHz to $329 at 700MHz, and TM3200 prices range from $65 at 333MHz to $89 at 400MHz (all for 1,000-unit quantities). For more information, go to *www.transmeta.com.*

Pentium III processors in MMC-2 cartridges with a north bridge, but that feature increases the TDP to 12.8W for the 500/600MHz mobile Pentium III and 19.1W for the 600/750MHz mobile Pentium III.

There are two clock-frequency numbers for each mobile Pentium III processor because they automatically reduce their core voltage and clock rate when unplugged from AC power, a feature Intel calls SpeedStep. For example, the 500/600MHz mobile Pentium III normally operates at 600MHz and 1.35V on AC power, but it steps down to 500MHz and 1.1V on batteries. Likewise, the 600/750MHz mobile Pentium III normally operates at 750MHz and 1.6V on AC power; however, it then steps down to 600MHz and 1.35V on batteries. Table 2 compares the specifications of Intel's and Transmeta's mobile processors for PC notebooks.

The differences between Intel's TDP specifications and average-power estimates are roughly an order of magnitude, which implies the average-power figure is based on a 10% duty cycle. ZD Media's eTesting Labs (formerly ZD Labs) told MDR that BatteryMark does indeed leave a system in idle states about 80% of the time, because that's how ZD Media's engineers think real people use notebook computers. So, as Transmeta alleges, BatteryMark's light duty cycle could explain the gap between Intel's average and worst-case power numbers. Figure 3 shows a power-consumption trace of the 500/600MHz mobile Pentium III in battery mode (500MHz).

The Quest for Better Benchmarks

The truth about Intel's and Transmeta's power-consumption claims is more elusive, however. For one thing, Intel didn't base its average-power estimates solely on BatteryMark. The company tested a wide range of desktop PC applications, as did Transmeta.

Not by coincidence, one application Intel tested was a DVD movie player, which is Transmeta's favorite demo. Playing a DVD movie on a 600/750MHz mobile Pentium III at 600MHz consumes an average of less than 2W, says Intel, and the same task consumes less than 1W on a 500/600MHz mobile Pentium III at 500MHz. But the screen photo in Figure 4 (supplied by Intel) traces the latter processor during DVD playback in battery mode, and it appears to show average power consumption in the 2.3W range. And Intel's TDP specifications clearly indicate that, to avoid meltdowns, system engineers must design for brief periods of much higher power consumption.

Unfortunately, Transmeta has been less forthcoming with power-consumption benchmarks than Intel. Transmeta criticizes Intel's BatteryMark score but won't release one of its own, saying that conventional tests like BatteryMark don't yield accurate results, because of the TM5400's unique LongRun technology. LongRun can vary the chip's core voltage from 1.1V to 1.65V and the clock frequency from 200MHz to 700MHz in 33MHz increments—all while running on battery power and in

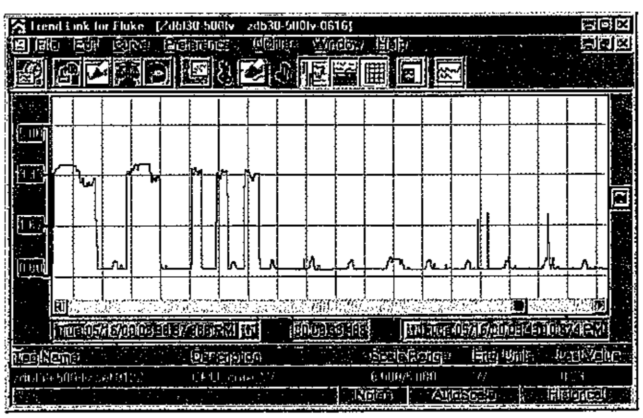


Figure 3. This power-consumption trace shows a 500/600MHz mobile Pentium III processor running the ZD Media BatteryMark 3.0 program, which keeps the CPU idle most of the time. That allows Intel's QuickStart power manager to reduce average power consumption well below 3W.

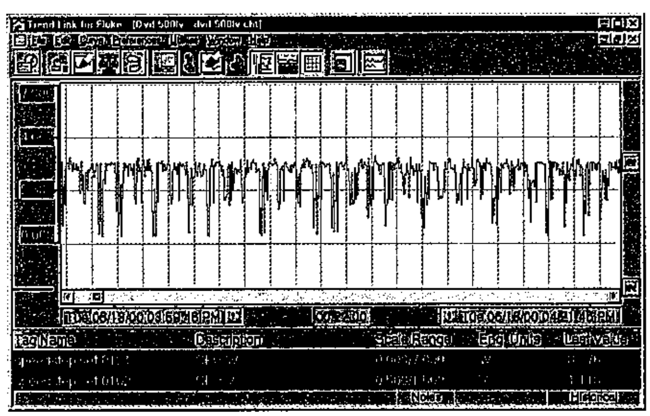


Figure 4. This trace shows a 500/600MHz mobile Pentium III processor playing a DVD movie in battery-optimized (500MHz) mode. Compared with the similar trace from Transmeta in Figure 2, the Intel processor appears to be consuming at least twice as much power—even without a north bridge, which would add about 4W.

Transmeta Explains LongRun

The last mysteries of Transmeta's LongRun technology were explained in a presentation at **Embedded Processor Forum** last month by Marc Fleischmann, the company's director of low-power programs. Although LongRun is somewhat less sophisticated than we imagined after Transmeta's public announcement in February, it is nonetheless effective.

Marc Fleischmann, Transmeta's director of low-power programs, explains LongRun at EPF2000.

At that time, Transmeta said LongRun scales a Crusoe processor's core voltage and clock frequency up or down in response to software demands, allocating just enough performance to handle the varying workload while conserving power. That sounds like a neat trick, but we wondered how LongRun could tell the difference between a true workload and a tight event loop that's simply waiting for something to happen. Answer: it can't. At least, not without a clue from the operating system in the form of an idle command.

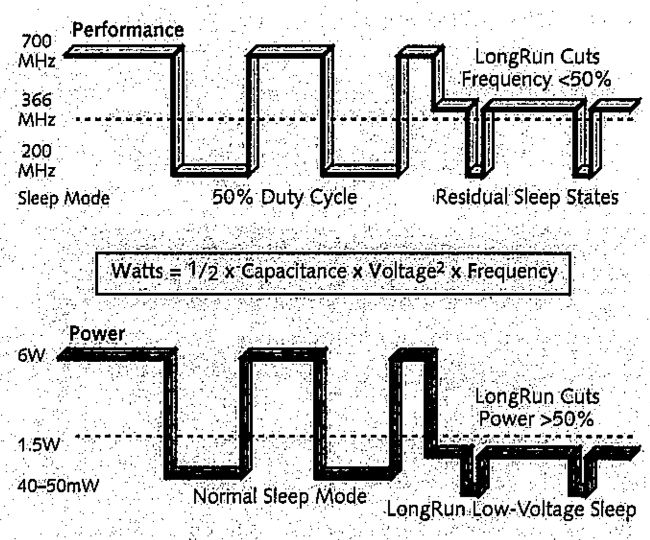
To conserve power, modern operating systems periodically issue idle commands to the CPU during brief periods when the need for processing power is low. Those periods might occur between the frames of an MPEG video stream, or even between a user's keystrokes. The idle command triggers the CPU's power-saving mode. The CPU goes to sleep until it needs to process an interrupt, then wakes up.

It turns out that Transmeta's code-morphing (x86 emulation) software constantly tracks the amount of time the CPU spends in sleep mode and uses that information to help LongRun regulate the chip's core voltage and clock frequency. For example, if the code-morphing software discovers the CPU is asleep half the time (e.g., a 50% duty cycle), it tells LongRun to cut the chip's voltage and frequency by a little less than 50%—say, 366MHz in the case of a 700MHz TM5400. As the figure below shows, that leaves enough performance to handle the software workload while boosting the duty cycle to near 100%.

By itself, reducing the clock rate would save little or no power, because the CPU is now working twice as hard at half the frequency to do the same amount of work. But LongRun also reduces the core voltage, which significantly cuts power consumption. That's because $W = {}^1/_2CV^2F$, where W is watts, C is capacitance, V is voltage (squared), and F is frequency. Therefore, power consumption drops faster than the linear reduction in frequency.

The CPU still gets a few catnaps after the clock-rate adjustment, because LongRun chooses a clock frequency that leaves some performance headroom. During those naps, the TM5400 enters a special low-voltage sleep mode that reduces power consumption to 40–50mW. The TM5400 consumes even less power in this mode than it does during the normal sleep mode.

LongRun is a clever and innovative approach to power management that does have the effect of scaling power consumption to software demands. And unlike AMD's similar PowerNow feature (see *MPR 5/1/00-05*, "AMD's K6 Family on the Move"), LongRun requires no modifications to the BIOS or operating system, because it takes advantage of existing power-management technology.



response to software workloads, unlike SpeedStep (see sidebar "Transmeta Explains LongRun"). The TM5400 would probably fare better with tests that simulate a heavier workload than BatteryMark, because LongRun could scale the core to some intermediate voltage and frequency within its broad range. A mobile Pentium III with SpeedStep would, however, be limited to its single battery-mode voltage and frequency.

On the other hand, a mobile Pentium III is likely to deliver more performance than a TM5400, and not just because the TM5400 has to emulate the x86. At its lowest LongRun-controlled power level of 1.1V, the 700MHz

TM5400 cuts back its clock frequency to a pedestrian 200MHz. At that same voltage, the 500/600MHz mobile Pentium III sprints at 500MHz.

We agree with Transmeta that existing power-consumption and performance benchmarks aren't the best way to evaluate the TM5400's unique abilities. Still, it would be nice to have more data points. Our experiments with Transmeta's power-monitoring system lead us to believe that the brief 6W power spikes we observed roughly correspond to Intel's TDP ratings, and that the TM5400's average power consumption is indeed in the 1.5W range. If our casual observations are confirmed by more rigorous tests on the Crusoe-based notebook computers soon to hit the market, Transmeta's promise of "all-day computing" could be realized.

One good sign is that Transmeta has joined EEMBC (EDN Embedded Microprocessor Benchmark Consortium) to help define a new suite of power-consumption tests and is working with other benchmarking organizations to refine their existing suites. Those efforts could benefit all CPU vendors, not just Transmeta. As more CPU architects turn to unusual techniques like LongRun to prolong battery life, power-consumption benchmarks will need to get more sophisticated—and now is not too early to start. ◇

EXHIBIT 6

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MAY 29, 2000

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BUSH Q&A
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HOT GROWTH COMPANIES

THE 100 BEST SMALL COMPANIES

PAGE 1?8

Linda McMahon, CEO, World Wrestling Federation; with WWF wrestler Kane

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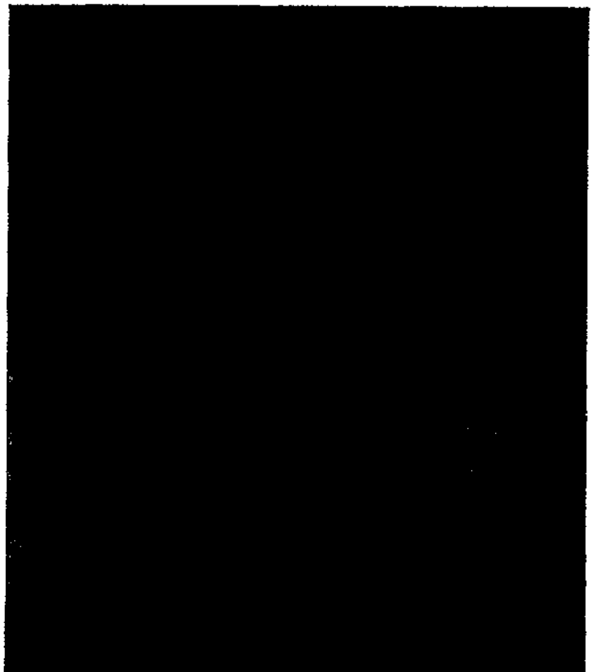
SEMICONDUCTORS

A SILICON CHAMELEON CHALLENGES INTEL

Transmeta's chips are fast, cheap—and upgradeable

David R. Ditzel knew he had pulled off a public-relations coup when no fewer than three CNN news crews, each with its own satellite-TV van, showed up last Jan. 19 for the unveiling of his company's super-secret chip. The chief executive of startup Transmeta Corp. had waited nearly five years for that moment. But even he was stunned by the turnout. So many newshounds came sniffing that Transmeta executives could spend only 15 minutes with each reporter. Starting at noon that day and continuing for the next 72 hours, the company's Web site was one of the 10 most visited places on the Internet, and Ditzel received hundreds of phone calls and e-mails. "It took two days for it all to sink in," he recalls.



DITZEL: *Investors include Compaq, Sony, and Samsung*

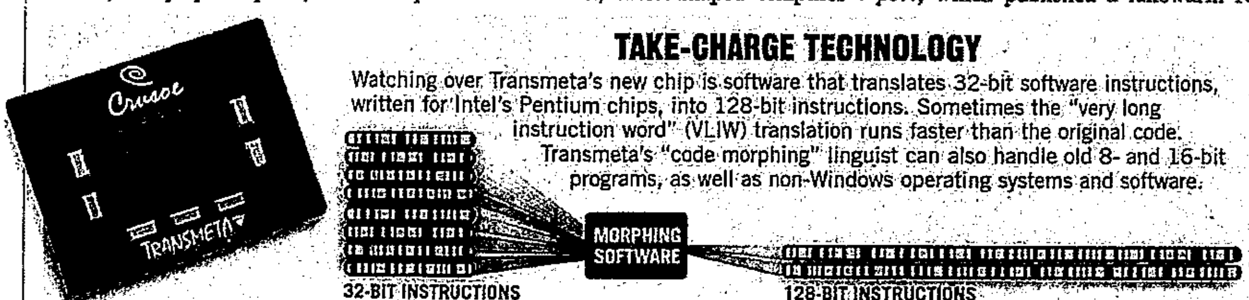
Now, the hoopla has started up again. Some top names in the electronics industry have kicked in $88 million to help Transmeta begin producing its speedy Crusoe processors. Sony, Gateway, Compaq, and America Online have all bought a stake in Transmeta. And now it's just started shipping in volume. By late June, the first Crusoe-based notebook PCs, handheld computers, and information appliances should begin showing up from companies such as IBM, Compaq Computer, former chipmaker S3 Corp., and Taiwanese giant Quanta Computer. These gizmos will run on batteries far longer than any predecessors. They could be smaller and lighter, too. "Transmeta's chips let us consider whole new market segments," says Andrew L. Wolfe, chief technology officer for S3, which plans this fall to unveil a 2-lb., tablet-shaped computer that can surf the Web wirelessly.

Why all the excitement? Until now, designers of mobile PCs and portable gadgets faced a frustrating conundrum: There are a half-dozen low-power processors on the market, from suppliers such as Hitachi Ltd. and Mips Technologies Inc., but these chips can't handle Windows software. And while Intel Corp.'s chips are adept at Windows, they gulp so much power that batteries usually last only a few hours. "People are tired of their batteries running out, tired of shoulder burn from heavy laptops," Ditzel says.

ON THE FLY. For its alternative, Transmeta relies on some digital trickery. Strictly speaking, its design is not compatible with Intel's Pentiums, which process instructions 32 digital bits at a time. Transmeta's circuits gobble instructions in 128-bit chunks, a technique called very long instruction word (VLIW). To pull that off, the chip's processing engine is wrapped in a silicon-and-software envelope that translates Pentium instructions, on the fly, into VLIW code. The upshot: A power-stingy 700-megahertz Crusoe can run Windows programs as fast as a 500-MHz Pentium III, the current champ in laptops. Yet Crusoe chips are smaller and have fewer transistors, so they cost as much as 50% less.

What's more, unlike any other microprocessor, Transmeta chips can be upgraded with software to remain on the cutting edge for years at a stretch. No longer will road warriors have to keep buying new laptops to get the latest gee-whiz features. Instead, they'll simply download VLIW software to acquire new capabilities.

Not everyone considers Transmeta a shoo-in, however. Among the skeptics is the closely read *Microprocessor Report*, which published a lukewarm re-



PHOTOGRAPH BY RICHARD MORGENSTEIN; GRAPHIC BY LAUREL ALLENBERG

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WHERE TRANSMETA SHOWS POTENTIAL

Transmeta has yet to announce its customers and their plans, but here are some that experts expect

COMPAQ COMPUTER An investor in Transmeta, the No.1 PC maker may use the new chips for a handheld PC.

GATEWAY Also a Transmeta investor, Gateway will probably deliver Transmeta-powered PCs, Web terminals, and wireless Web tablets.

AMERICA ONLINE The online giant is exploring several non-PC devices. Yet another Transmeta investor, AOL could also market Web gizmos from Gateway and others.

S3 This former maker of graphics chips has bet its future on Internet appliances. The first will be a Web pad using a Transmeta chip and Linux software.

IBM Big Blue, which makes Transmeta's chips in an ultramodern factory, will also use the chips for IBM laptops and other systems.

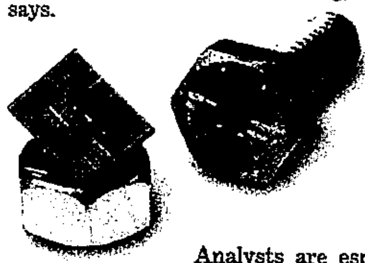
view, wondering if Transmeta was setting its prices a little too high. And Joseph J. Byrne, an analyst with market researcher Dataquest Inc., says Intel has the resources to paint Transmeta into a corner while it develops something comparable. Indeed, when it comes to challenging Intel, history is not encouraging. A half-dozen have tried. Only longtime nemesis Advanced Micro Devices Inc. (AMD) has made a lasting dent and now enjoys a 17% share of the market for Intel-type chips.

Don't pester Ditzel with such details. The 43-year-old entrepreneur, who once worked for Bell Labs and headed processor development at Sun Microsystems Inc. for eight years, has raised some $188 million from venture capitalists and Microsoft Corp. cofounder Paul Allen, and the new investor-customers. Buyers of the chips, which are manufactured by IBM, are playing their own game of say-little, to whet expectations about upcoming products. But analysts figure there are some pretty safe bets (table), such as portable systems from Compaq and IBM.

Besides lots of money and big-name customers, Ditzel has assembled a team of high-profile engineers and execs. One is James N. Chapman, who spent 11 years at Intel and then flogged sales of Intel-compatible chips at Cyrix Corp. Another example: Linus Torvalds, the legendary author of the popular Linux operating system. With such talent, Ditzel declares, "we have no qualms about competing in the market."

The opportunity is enormous. Transmeta's high-end chip, dubbed the Crusoe TM5400, is priced from $120 to $300, depending on configuration, and is aimed at laptops, the fastest-growing segment of the PC business. The simpler TM3200, costing $65 to $90, is meant for information appliances, a still-nascent market that could explode over the next few years. All told, the potential for Crusoe chips could top 160 million units by 2003. Grabbing even a 10% share would

mean billions in revenues. And some observers figure Transmeta could do far better. "This is the first truly innovative development in processors in the last 12 years," says Drew Peck, an analyst at Boston brokerage SG Cowen & Co. Even more enthusiastic is Robert A. Enderle, a chip watcher at Giga Information Group Inc. "Transmeta has the potential to overthrow the king," he says.



Transmeta's rivals are taking notice. Intel has pledged to deliver a Pentium chip this summer that matches Crusoe's power consumption

THE POTENTIAL FOR CRUSOE CHIPS COULD TOP 160 MILLION UNITS BY 2003

Analysts are especially intrigued by the clever software layer that translates Intel instructions into VLIW. This linguist could easily handle other types of software code as well. So one computer could run not only Windows but also Macintosh programs and Sony PlayStation games. In effect, the Crusoe is a silicon chameleon. This "software microprocessor," Ditzel stresses, gives Transmeta significant competitive advantages. It can take years to revise the complex silicon circuits on an Intel or AMD chip. But Crusoe designs can be upgraded with simple keystrokes. Case in point: A customer in Japan found a bug in an early Crusoe version. Transmeta engineers quickly wrote a fix, then zapped the new code to the customer electronically. "We essentially sent them a new microprocessor over the Internet in a week," Ditzel says. "It blew them away."

So far, rivals are hardly quaking, but they're definitely taking notice. AMD Senior Vice-President Robert R. Herb praises Transmeta's technology but cautions that surviving in the cutthroat market for Intel-compatible chips will be tough. And Transmeta can't get by with just a snappy processor, he adds: It also needs to develop the usual companion chips and development tools for customers. James R. Edwards echoes that point. He's a marketing manager at National Semiconductor Corp., which fled PC processors last year but continues to make a special-purpose chip for info appliances. Called Geode, this chip has most of the required silicon companions built in. Still, the lack of Transmeta support chips didn't stop S3 from chucking Geode in favor of Crusoe.

Intel won't comment on Transmeta. But at its Apr. 27 meeting with Wall Street analysts, Intel pledged to deliver a Pentium this summer that matches Crusoe's power consumption. That, sniffs Chapman, is an empty promise to keep customers from jumping ship. Could be. On the other hand, if Transmeta does begin stealing laptop customers en masse, Intel will certainly unleash a ferocious counterattack. For Transmeta, too much success could precipitate a backlash. To survive, Ditzel will need all the lavish publicity, capital, and talent—and cunning—he can muster.

By Andy Reinhardt in Santa Clara, Calif.

EXHIBIT 7

Seiko Epson and Transmeta Announce Future Cooperation In The Development of Crusoe-Related Technology

Seiko Epson and Transmeta Announce Future Cooperation In The Development of Crusoe-Related Technology

For Immediate Release

SANTA CLARA, California (June 21, 2001) and TOKYO, Japan (June 22, 2001) -- Seiko Epson Corporation and Transmeta Corporation (NASDAQ: TMTA) today announced that they have agreed to cooperate in the future in the development of semiconductor technology related to Crusoe microprocessors, a family of energy-saving microprocessors developed by Transmeta primarily for mobile computing systems.

In early 2000, Transmeta unveiled its revolutionary Crusoe microprocessors, a family of x86-compatible microprocessors whose low power consumption enables long battery life for mobile computers. The Crusoe microprocessor has since been used in notebook PCs by many major computer manufacturers. It has also been recognized for its suitability for personal digital assistants, Internet appliances, and other systems.

Seiko Epson's semiconductor business is based on the concept of "energy-saving" technology, and one of its focuses is on developing semiconductor products specifically for mobile information equipment. Mobile information equipment calls for ICs with not only low power consumption but also space efficiency to enable smaller equipment. To fulfill these requirements, Seiko Epson develops "energy-saving," low-power-consuming products by utilizing core technologies: in the IC manufacturing process, processing technology characterized by low power consumption and high integration; and in the mounting stage, mounting technology aimed at further weight and size reduction.

To build upon their respective strengths, Seiko Epson and Transmeta have agreed to cooperate in the future in the development of semiconductor technology related to energy-saving Crusoe microprocessors for mobile equipment. The elements of the relationship are as follows:

- Seiko Epson has assigned to Transmeta a limited portion of its patents and patent rights relating to microprocessor technology.

- Seiko Epson and Transmeta will collaborate and share information about their "energy-saving" technologies in an effort to develop higher-level peripheral chipsets and other devices for Crusoe microprocessors.

- Seiko Epson and Transmeta will establish a cooperative relationship toward the development of a technology partnership or alliance in the Internet appliances field.

- Seiko Epson and Transmeta will explore the possibilities of further cooperation and technical exchange in other technology areas.

Seiko Epson and Transmeta will continue to strengthen their cooperative ties in the development of semiconductor products for mobile information equipment.

Saburo Kusama, President of Seiko Epson Corporation, said "Energy-saving technology, at which Seiko Epson excels, is important and essential technology for development in the field of mobile information equipment. We are looking forward with keen anticipation to further expansion of the market, as well as rapid progress in semiconductor technology that is the basis of mobile information equipment, by the cooperative use of the remarkable technologies owned by the two respective companies."

"Transmeta is very pleased to announce this significant relationship with an established and respected technology leader like Seiko Epson," said Mark K. Allen, President and Chief Executive Officer, Transmeta Corporation. "We regard the patent rights to have substantial strategic value toward the development of Crusoe technology, and we are optimistic that this collaborative effort with Seiko Epson will contribute to the development of new energy-saving computing technologies."

About EPSON

Seiko Epson Corporation (EPSON) started its operation in 1942 as a manufacturer of SEIKO watches. Since then, the company's operations have expanded to encompass the entire range of information-related equipment, including the development, manufacture, and sale of EPSON printers, personal computers, multi-media projectors, electronic devices and components, etc. The EPSON group takes at heart its management philosophy of maintaining its worldwide reputation as a reliable and respectable company. Seiko Epson Corporation currently has 122 affiliates and representative offices in 38 countries and recorded consolidated annual sales of JPY 1,340.9 billion for the fiscal year ending March 31, 2001.

Additional information is available on the Internet at: http://www.epson.co.jp/e/ae/.

About Transmeta Corporation

Transmeta is a publicly traded company (NASDAQ: TMTA) located in Santa Clara, California. Transmeta develops and sells software-based microprocessors and develops additional hardware and software technologies that enable computer manufacturers to build computers that simultaneously offer long battery life, high performance and x86 compatibility. Transmeta's family of Crusoe microprocessors is targeted at the notebook and Internet appliance segments of the mobile Internet computer market, as well as ultra-dense servers. For more information visit Transmeta on the web at www.transmeta.com.

Cautionary Statement for Transmeta Investors

This release contains forward-looking statements, which are made pursuant to the safe harbor provisions of the U.S. Private Securities Litigation Reform Act of 1995. Forward-looking statements are generally preceded by words such as "plans," "expects," "believes," "anticipates" or "intends." Investors are cautioned that all forward-looking statements in this release involve risks and uncertainty that could cause actual results to differ materially from current expectations. We urge investors to review in detail the risks and uncertainties described in Transmeta's recent filings with the United States Securities and Exchange Commission, including specifically our recent Form 10-K and our most recently filed Form 10-Q.

EPSON is a trademark of Seiko Epson Corporation. Transmeta and Crusoe are trademarks of Transmeta Corporation. Any other product names are used for identification purposes only and may be trademarks owned by other companies.

EXHIBIT 8

The JFTC rendered a recommendation to Intel K.K.

The Japan Fair Trade Commission (JFTC), March 8, 2005, rendered a recommendation to a Japan-based company, Intel Kabushiki Kaisha (IJKK), a wholly-owned subsidiary of Intel International (a wholly-owned subsidiary of Intel Corporation, Santa Clara, CA, USA). The recommendation requires IJKK to cease and desist its conducts which violate Section 3 of the Antimonopoly Act (Private Monopolization). The JFTC has been investigating since last April.

The Facts-Findings in the Recommendation

IJKK, since May 2002, has made the five major Japanese OEMs[1] refrain from adopting competitors' CPUs[2] for all or most of the PCs manufactured and sold by them or all of the PCs that belong to specific groups of PCs referred to as 'series', by making commitments to provide the five OEMs with rebates and/or certain funds referred as 'MDF' (Market Development Fund) in order to maximize their MSS[3], respectively, on condition that

(a) the Japanese OEMs make MSS at 100% and refrain from adopting competitors' CPUs.
(b) the Japanese OEMs make MSS at 90%, and put the ratio of competitors' CPUs in the volume of CPUs to be incorporated into the PCs manufactured and sold by them down to 10%; or
(c) the Japanese OEMs refrain from adopting competitors' CPUs to be incorporated into PCs in more than one series with comparatively large amount of production volume to others.

Based on the facts mentioned above, the ratio of the sales volume by AMD Japan and Transmeta USA among Total Domestic CPU Sales Volume decreased from approximately 24% in 2002 to approximately 11% in 2003.

By means of such conducts, IJKK has substantially restrained the competition in the market of CPUs sold to the Japanese OEMs, by acting to exclude its competitors' business activities related to the sales of CPUs to the five OEMs.

Summary of Measures Recommended

(1) IJKK, when selling Intel's CPUs to the Japanese OEMs, shall terminate such conducts which have been engaged by IJKK since May 2002 as; with respect to the CPUs incorporated into the PCs manufactured and sold by the Japanese OEMs, by making commitments to provide the Japanese OEMs with the rebates and/or funds on condition that, as mentioned above, the Japanese OEMs refrain from adopting competitors' CPUs to be incorporated into all or most of the PCs which are manufactured and sold by them.

---

1 Japanese manufacturers of PCs of which head offices are located in Japan.
2 x86 series central processing units.
3 MSS is the ratio of the CPUs manufactured and sold by Intel ('Intel's CPUs') in the volume of CPUs to be incorporated into the PCs which are manufactured and sold by an OEM.

(2) IJKK shall notify the following matters to all the Japanese OEMs with which IJKK deals, and shall also make them known to its employees thoroughly.

a) Measures taken by IJKK based on (1) above

b) IJKK, when providing the Japanese OEMs with such rebates and/or funds, has no intention to set condition which lead to exclude competitors' CPUs out of the PCs which are manufactured and sold by the Japanese OEMs

c) IJKK has already terminated the conduct to make a Japanese OEM not adopt competitors' CPUs in more than one groups of PCs, each of which has comparatively large amount of production volume to others, thereby making all the PCs in those groups of PCs at that OEM incorporate Intel's CPUs, by making a commitment to provide it with the rebates and/or funds on condition that the Japanese OEM change to Intel's CPUs competitors' CPUs previously incorporated into the PCs in those groups of PCs, and that it keep using Intel's CPUs in all the PCs in those groups of PCs.

(3) IJKK, from now on, shall not exclude the business activities of the competitors for the sales of CPUs by employing following conducts:

a) The conduct to restrict the ratio in the volume of competitors' CPUs to be incorporated into the PCs manufactured and sold by a Japanese OEM at 10 percent or less, by making a commitment to provide the Japanese OEM with the rebates and/or funds on condition that it make MSS at 90% or more and maintain MSS at such level

b) The conduct to, without justification, make a Japanese OEM not adopt competitors' CPUs to be incorporated into PCs in more than one groups of PCs, each of which has comparatively large amount of production volume to others, thereby making all the PCs in those groups of PCs at that OEM incorporate Intel's CPUs, by making a commitment to provide the Japanese OEM with the rebates and/or funds on condition that it change to Intel's CPUs competitors' CPUs previously incorporated into the PCs in those groups of PCs, and that it keep using Intel's CPUs in all the PCs in those groups of PCs.

(4) IJKK shall take measures to operate (i)Antimonopoly training for officers of sales department and their staffs engaged in promoting and selling CPUs, and (ii)periodical audits by legal section, thereby ensuring the conduct mentioned above in (3) shall not be caused hereafter.

<u>Due Date of Acceptance or Rejection of the Recommendation</u>

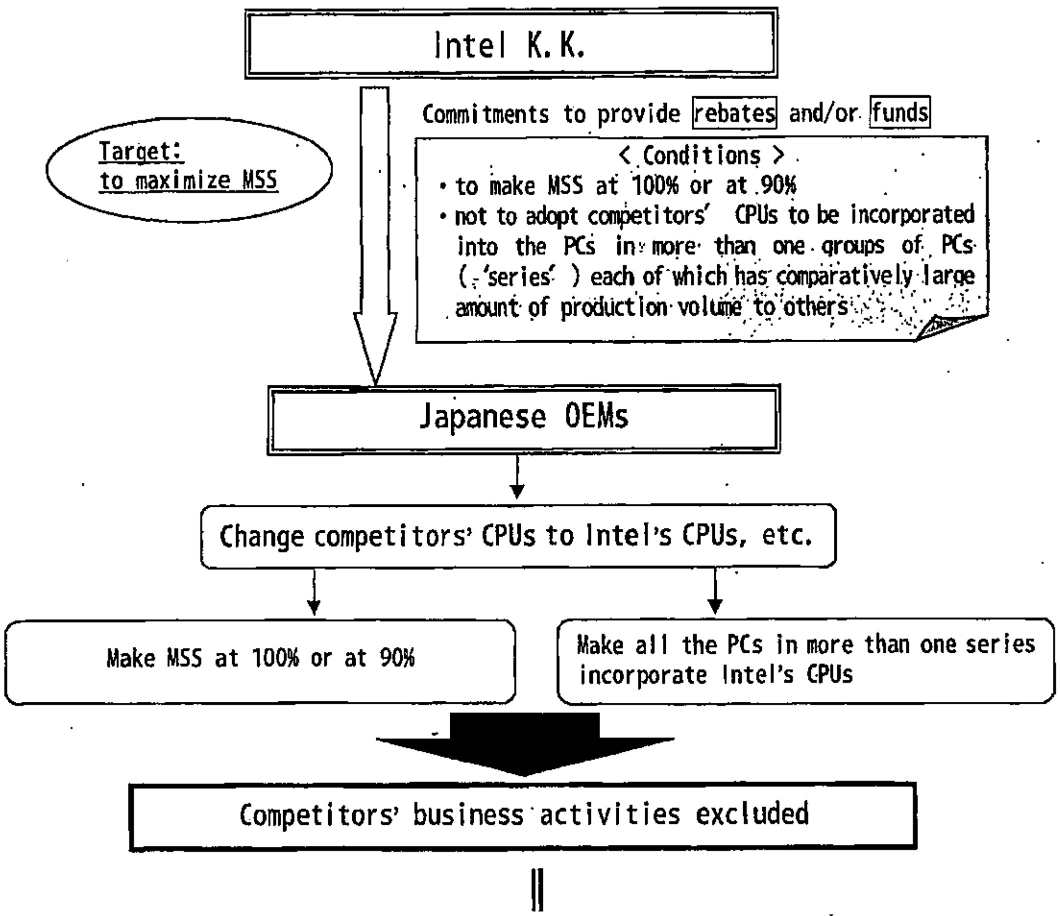
March 18, 2005

(If the recommendation is accepted, the JFTC will issue a decision, a legally binding order with the same corrective measures as those in the recommendation. Otherwise, the JFTC will initiate a hearing procedure.)

Contact point: Third Investigation Division, Investigation Bureau
03-3581-3345

Exhibit

Outline of Intel K.K.'s conducts



Share of competitors' CPU declined

	2003	2004
Share of competitors' CPU (i)	24%	11%

(i) Ratio of the sales volume of CPUs sold, either directly or through dealers, to the Japanese OEMs by AMD Japan and Transmeta USA in the total sales volume of CPUs sold by IJKK, AMD Japan and Transmeta USA (CPUs sold by IJKK, AMD Japan and Transmeta USA amount to almost all the CPUs sold in Japan.).

EXHIBIT 9

March 9, 2005

Japan Says Intel Violated Antimonopoly Law

By TODD ZAUN

TOKYO, March 8 -The Fair Trade Commission in Japan ruled on Tuesday that the Intel Corporation violated the country's antimonopoly law in the way it sold semiconductors and ordered the company to stop some of its sales practices.

Intel took issue with the finding and said it was considering how to respond.

The commission said Intel used unfair business practices to persuade five Japanese personal computer makers, including Sony and Toshiba, to stop or limit their purchases of microprocessors from two Intel rivals, Advanced Micro Devices and the Transmeta Corporation.

The action against Intel came 11 months after the commission began its investigation with a raid on the company's Japanese offices. Fair trade authorities said that since May 2002, Intel offered discounts and incentives to computer makers that were contingent on promises that those companies either cease, or strictly limit, purchases from other chip makers.

Intel said in a statement that it regarded its practices as fair and lawful. The company has 10 days to decide whether to appeal. If it does, the case would go through the commission's judicial review process.

"There is a broad consensus that competition regulators should only intervene where there is evidence of harm to consumers," D. Bruce Sewell, Intel's vice president and general counsel, said in the statement. "It is apparent the J.F.T.C.'s recommendation did not sufficiently weigh these important principles."

The ruling, which does not carry a fine, was the second action by Japanese competition regulators against a major American high-technology company in the last year. In July, the commission ordered Microsoft to remove a clause in its licensing contracts that was intended to protect it from patent suits.

Intel has about 90 percent of the Japanese market for microprocessors, with the remainder split between Advanced Micro and Transmeta. That compares with an 80 percent market share for Intel worldwide.

In the ruling, regulators did not ask Intel to stop offering volume discounts or other incentives to computer makers, but it did order the company to stop tying those discounts to promises to stop buying rival brands.

In one case, Intel forced a computer maker to buy all of its semiconductors from Intel or lose rebates that had been offered, the commission said without identifying the manufacturer.

Regulators argued that Intel's sales methods were unfair because the stipulations virtually assured that

computer companies would severely limit purchases from rivals. Intel's brand power with consumers and its overwhelming market share in Japan mean computer makers have little choice but to buy a large number of their chips from Intel, and losing the discounts on those purchases would be costly, they said.

The commission determined that Intel's practice limited competition and thus was likely to drive up the cost of computers for consumers, said Hiroshi Yamada, a commission official who briefed reporters on the decision.

"The company urged the five computer makers not to buy products from rivals in order to raise its own market share," Mr. Yamada said.

The combined Japanese market share of A.M.D. and Transmeta dropped by more than half from 24 percent in 2002 to 11 percent in 2003, the commission said. Intel accounted for the remainder of the market, so its share rose to 89 percent from 76 percent in the period.

A.M.D. has cited Intel's sales practices for its dwindling market share in Japan and applauded the ruling.

"It's a clear determination by the F.T.C. that Intel has been abusing a dominant position to limit competition," Thomas M. McCoy, executive vice president for legal affairs at A.M.D., said in an interview here.

EXHIBIT 10

Intel News Release

Intel Agrees To Comply With JFTC Recommendation; Disagrees With Findings Of Fact

SANTA CLARA, Calif., March 31, 2005 - Intel Corporation today announced that its Japanese subsidiary, Intel K.K. (IJKK), is accepting a Recommendation from the Japan Fair Trade Commission (JFTC) dated March 8, 2005. Although IJKK accepts the Recommendation, the company does not agree with the facts underlying the JFTC's allegations and the application of law in the Recommendation. IJKK continues to believe its business practices are both fair and lawful, but the company believes that the cease and desist provisions of the Recommendation will not impair it from continuing to meet customer requirements.

"Intel respectfully disagrees with the allegations contained in the Recommendation, but in order to continue to focus on the needs of customers and consumers, and continue to provide them with the best products and service, we have decided to accept the Recommendation," said Bruce Sewell, vice president and general counsel for Intel. "We believe the Recommendation's cease and desist provisions define a workable framework that enables us to continue to provide competitive pricing to our customers, and benefits consumers and the Japanese economy. We do not accept the Recommendation's allegations in its fact findings and the application of law. We believe the allegations misinterpret important aspects of our business practices and fail to take into account the competitive environment within which Intel and its customers compete."

About Intel
Intel, the world leader in silicon innovation, develops technologies, products and initiatives to continually advance how people work and live. Additional information about Intel is available at www.intel.com/pressroom.

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EXHIBIT 11

REDACTED